A New Methodology to Reverse the Power Flow in a Single Phase AC System by Using a D-SSSC

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***Abstract*-To avoid power crisis the distributed generators are very essential now-a-days. Generally distributed generators are connected in radial system. These radial systems are converted to looped or meshed network for improving the power transfer capability in the system. Power electronics converters are in need for the injection of power. Here a static series synchronous Compensator (SSSC) can be used as a replacement. So this type of SSSC is called D-SSSC. This scheme uses a Cascaded multi- level inverter which neglects the transformer and gives better efficiency. The looped network sometimes will be reversed the power flow operation. That time, the phases current are not considered in the earlier current phase locked loop control. Now we using voltage phase locked loop and current phase locked loop control can be neglected. Here in this proposed project work the voltage phase locked loop is presented and comparative study is shown using Simulink. The existing control strategy that is VPLL is dealt with PI controller. But it has some disadvantages like maximum overshoot, harmonics and more oscillation and settling time. In order to reduce these disadvantages the PID controller is used and a compared and presented for PI and PID controller in D-SSSC cascaded H-bridge to reverse the power flow.**

***Keywords*- Distributed static series synchronous compensator (DSSSC), phase locked loop (PLL), power flow control, Cascaded H-bridge, Proportional Integral (PI), Proportional Integral Derivative (PID) controller.**

I. INTRODUCTION

The conventional radial electrical distribution system will change to loop or even meshed system due to the deregulation of electrical system and connection of Distributed Generation to Medium and Low voltage in future. Controlling the power flow between two feeders from different substation by placing a D-SSSC in the connection point will be source of many advantages. These advantages will be voltage regulation, increasing reliability, loss reduction, avoiding congestion in cables and facilitating use of distributed generation. The main principle of D-SSSC operated without an external electric energy source as a series compensator whose output voltage is in quadrature and controllable independently of the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the transmitted active power. Electricity systems are very complex systems and are composed of numerous generators, transmission lines, and loads. The distributed power generations (DG's) is given more importance which is mainly connected to the distributed network. Most electrical networks are widely interconnected for economic reasons – optimum sharing of electrical power, optimum utilization of resources and deregulation of electric market. The conventional radial distribution network is not able to handle these demands and needs to change to loop or even meshed distribution network. Flexible AC transmission system (FACTS) is an emerging technology and its principal role is to enhance the controllability and the power transfer capability in ac systems [1]. FACTS technologies use switching power electronic devices to control the power flow i.e distributed static series compensator (DSSSC).

The DSSSC is able to inject a voltage in series to line to control the power flow between two feeders. In this method of power flow controlling, there are various advantages like voltage regulation, losses reduction, avoiding congestion in the feeders, load sharing between feeders and increasing reliability. The DSSSC injected voltage to the line can be arranged in order to reverse the power flow despite of the phase angle between substations. The DSSSC is directly connected to medium voltage network. The multilevel converter is used as a main topology omitting the heavy and bulky transformer. Among the multilevel topologies the cascade H-bridge is used as a desired topology [2]. The conventional control strategy uses the phase angle of line current by a phase locked loop and injects a voltage in phase to line current to maintain the DC bus voltage and a voltage in quadrature to line current for controlling the power flow. But when the power flow reverses, the line current PLL is not able to work properly due to the low and zero current at that point. This intern fails the whole control strategy [3]. In this work, we have proposed new control strategy in the distribution system for reversing the power flow. This strategy is based on tracking the phase of feeder voltage. The feasibility of this method to reverse the power flow is demonstrated through simulation results and PI controller is replaced by PID controller in order to reduce the maximum overshoot, steady state with less settling time. Due to this the total harmonic distortion (THD) of the compensator is reduced.

II.DISTRIBUTION STATIC SYNCHRONOUSSERIES COMPENSATOR SYSTEM MODELING

The conventional radial electrical distribution system will change to loop or even meshed system due to the deregulation of electrical system and connection of Distributed Generation to Medium and Low voltage in future. Controlling the power flow

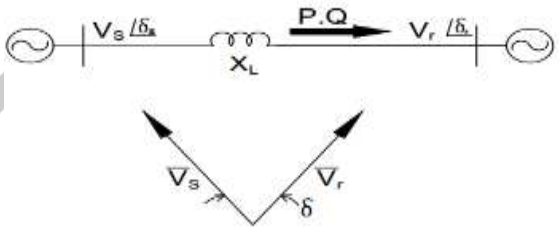
between two feeders from different substation by placing a D-SSSC in the connection point will be source of many advantages. These advantages will be voltage regulation, increasing reliability, loss reduction, avoiding congestion in cables and facilitating use of distributed generation. The main principle of D-SSSC operated without an external electric energy source as a series compensator whose output voltage is in quadrature and controllable independently of the line current for the purpose of increasing or decreasing the overall reactive voltage drop across the line and thereby controlling the transmitted active power. The D-SSSC may include transiently rated energy storage or energy absorbing devices to enhance the dynamic behavior of the power system by additional temporary real power compensation, to increase or decrease momentarily, the overall resistive voltage drop across the line [3].

Fig 3 Shows a simple transmission line with an inductive reactance (XL) Connecting a sending-end voltage source (Vs), and a receiving-end voltage source (Vr) respectively. The single line diagram of a simple transmission line real and reactive power (p and Q) flow at the receiving end voltage source are given by the expressions. Vs are the voltage magnitude of machine-1.Vr is the voltage magnitude of machine-2.□s and □r are the phase angles of the voltage sources VS and Vr, respectively.□□is the phase difference between these voltages. For simplicity, the voltage magnitudes are chosen such that VS = Vr = V and the difference between the phase angles is □= □s-□r. D-SSSC acts as capacitive impedance in two times of operation.

$$P = \frac{V_S V_R}{X_L}\sin(\delta s - \delta r) = \frac{V^2}{X_L}\sin\delta \text{ -------- (1)}$$

$$Q = \frac{V_S V_R}{X_L}(1 - \cos(\delta s - \delta r) = \frac{V^2}{X_L}(1 - \cos\delta) \text{ ------- (2)}$$

Once in the positive power flow controlling which the injected voltage is less than the difference voltages of receiving ends and second in the reversed power flow which the injected voltage is more than the difference voltages of sending ends. So when the power flow is going to reverse the injected voltage needs to change from inductive mode to capacitive mode. Therefore, the expressions for power flow given in equation (1) become



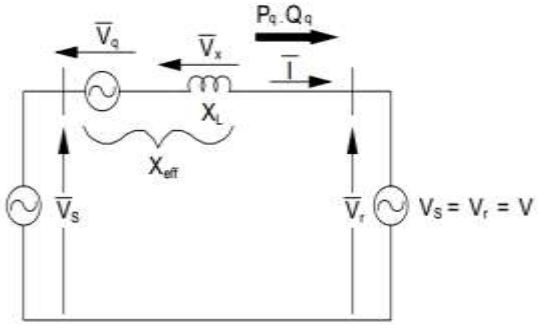
$$P = \frac{V_S V_R}{X_L}\sin\delta, \qquad Q = \frac{V_S V_R}{X_L}(1 - \cos\delta)$$

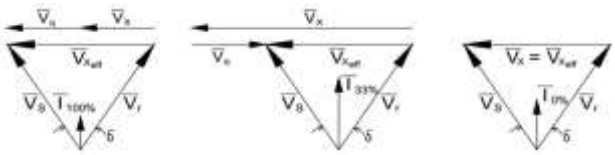
Fig 3. Power transmission system

$$P_q = \frac{V^2}{X_{eff}}\sin\delta = \frac{V^2}{X_L\left(1-\frac{X_q}{X_L}\right)}\sin\delta \text{ -------- (2a)}$$

$$Q_q = \frac{V^2}{X_{eff}}(1 - cos\delta) = \frac{V^2}{X_L\left(1-\frac{X_q}{X_L}\right)}(1 - cos\delta) \text{ ---------- (2b)}$$

Where *Xeff* is the effective reactance of the transmission line between its two ends, including the emulated variable reactance inserted by the injected voltage source of the SSSC. The compensating reactance, *Xq*, is defined to be negative when the SSSC is operated in an inductive mode and positive when this is operated in a capacitive mode.Fig4.shows an example of a simple power transmission system with an SSSC operated both in inductive and in capacitive modes and the related phasor diagrams. The line current decreases from Io% to I-100%, when the inductive reactance compensation.





$$P = \frac{V_S V_R}{X_{eff}} sin\ \delta, \qquad Q = \frac{V_S V_R}{X_{eff}} (1 - \cos \delta)$$

$$X_{eff} = X_L - X_q$$

Fig.4.A phasor diagram of SSSC operated in inductive and capacitive mode, *-Xq/XL,* increases from 0% to 100%. The line current increases from Io% to I33%, when the capacitive reactance compensation, *Xq/XL,* increases from 0% to *3%*.[4]

MATLB SYSTEM MODELING

The system consists of two generating machines along with transmission line and load as shown in figure 5 and 6 are VPLL PID and PI controller and Fig.7 CPLL PI controller The compensator is provided with a DC voltage source which helps in feeding or absorbing the active and reactive power from the system.[5]

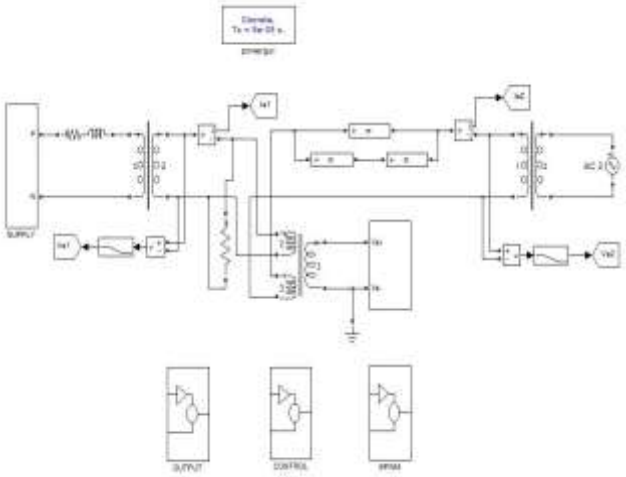


Fig.5 VPLL with PIDcontroller matlb system modeling.

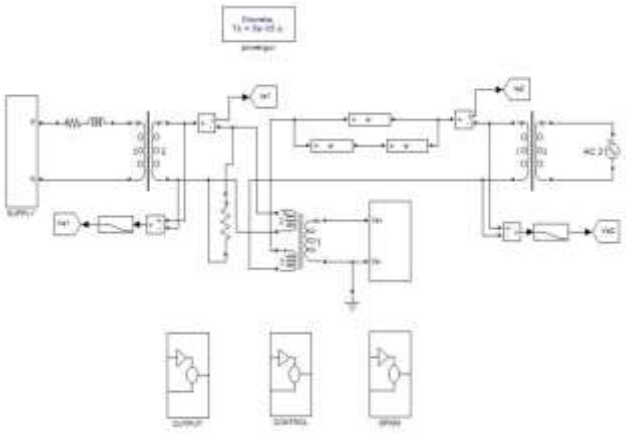


Fig.6 VPLL with PIcontroller matlb system modeling.

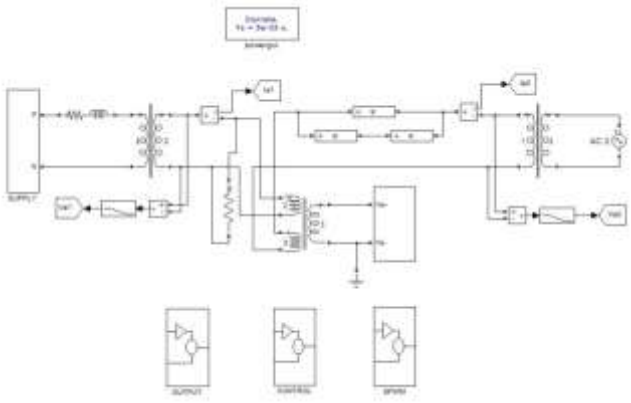


Fig.7.CPLL with PI controller matlb system modeling.

III.MULTILEVEL VOLTAGE SOURCE INVERTER USING CASCADED-INVERTERS WITH SEPARATED DC SOURCES

For a three-phase system, the output of three identical structure of single-phase cascaded inverter can be connected in either wye or delta configuration. Fig 8illustrates the schematic diagram of wye-connectedseven-level inverter using three H-bridge cells andthree SDCSs per phase, which will be usedto verify the concept of the optimized harmonic stepped-waveform technique. V_{AN} isvoltage of phase A, which is the sum of V_{a1}, V_{a2}, and V_{a3}.The same idea is applied to phase B and phase C. To synthesize seven-level phase voltage, three firing angles are required. Thesame three switching angles can be used in all three phase with delaying 0, 120, and 240 electrical degree for phase A, B, and C, respectively According to three-phase theory, line voltage can be expressed in term of two-phase voltages.The advantage of three-phase system is that all triplen harmonic components in the line voltage will be eliminated by one-third cycle phase shift feature. Therefore, only non-triplen harmonic components need to be eliminated from phase voltage. In single-phase nine-level waveform, for example, the 3rd, 5th, and 7th harmonics will be eliminated from output phase voltage. Compared to single-phase inverter, in three-phase nine-level inverter, the 5th, 7th, and 11th harmonics will be eliminated from output phase voltage. Thus, the 9th harmonic is the lowest harmonic component in phase voltage in single-phase system, while the 13th harmonic is the lowest harmonic component appearing in line voltage of three-phase system.as shown in fig. 9 VPLL and Fig. 10 CPLL THD simulation result.

IV.CONTROL STRATEGY

A **phase-locked loop** or **phase lock loop** (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. While there are several differing types, it is easy to initially visualize as an electronic circuit consisting of a variablefrequency oscillator and a phase detector. The oscillator generates a periodic signal. The phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is 'fed back'toward the input forming a loop.

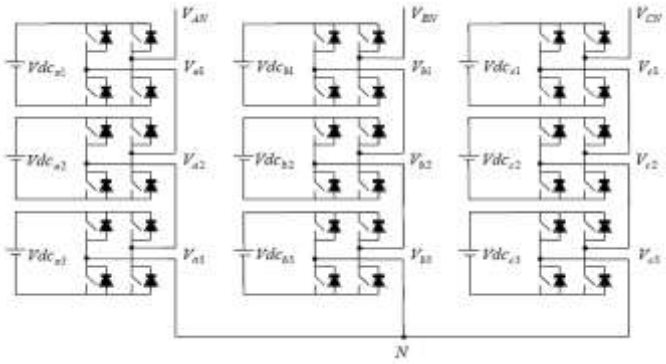


Figure8. Three-phase seven-level inverter using cascaded-inverters with SDCSs.

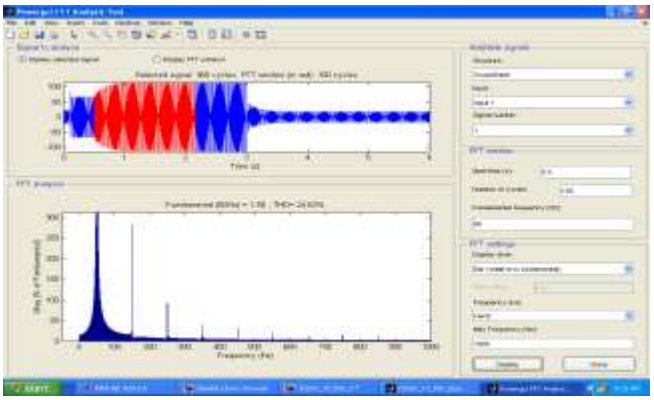


fig. 9 VPLL(PID) THD simulation result.

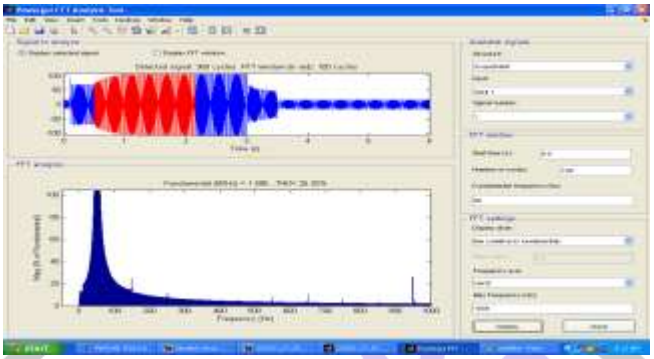


fig. 10 CPLL (PID) THD simulation result.

A PLL is a feedback system that includes a voltage control oscillation (VCO), phase detector, and low pass filter within its loop. Its purpose is to force the VCO to replicate and track the Frequency and phase at the input when in lock. The PLL is a control system allowing one oscillator to track with another. It is possible to have a phase offset between input and output, but when locked, the frequencies must exactly track. As a result of not including any auxiliary source power this strategy can control only the active or Reactive parts of power flow. This control strategy uses two control loop, one for maintaining the DC bus voltage at its reference value which produces the in phase part of injected voltage with the line current and the second loop, control the amount of power flowing the connected line which makes the quadratic part of injected voltage with current. The reference current, active or reactive power is compared with the actual value and passing through a PI controller generates the quadratic part amplitude. The power flow can be increased by acting DSSSC as additional capacitive impedance in series with the transmission line, and decreased by acting it as additional inductive impedance in series with the transmission line .In this control technique two PI controllers are used. One of the PI output controllers is used to identify the mode of operation. The reference DC bus voltage is compared with actual DC bus voltage using another PI controller the amplitude of in phase part of injected voltage is as shown in fig 11. But in crossing from the zero current for reversing the power flow the PLL is not able to produce the well results and lose the current phase track which causes thermal function of whole control system. So for solving this problem another control strategy is proposed which uses the phase of feeder voltage instead of current phase. As a result of not having the current phase, it is not possible to maintain the DC bus voltage by controlling then phase part of injected voltage directly. So the new control strategy which is showed in Fig. 7 and 8.Uses the variable DC bus voltage. The active power or current is compared to the actual value and passing a PI controller the voltage reference is produced. In this control strategy, the DC bus voltage is not fixed and varies by the changing in power flow while the modulation index is fixed at (0.9). This reference is compared with the actual DC bus voltage value and using another PI controller, a phase displacement γ is obtained. As a result of having one of feeder voltages close to the injected voltage, it is easy to use it as a reference for phase synchronization.

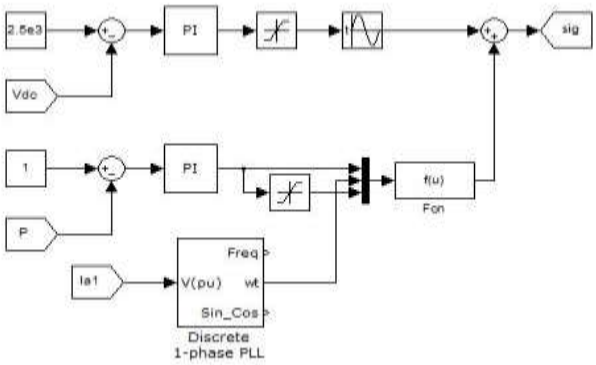


Figure 11. Power flow control with current phase locked loop (With PI controller)

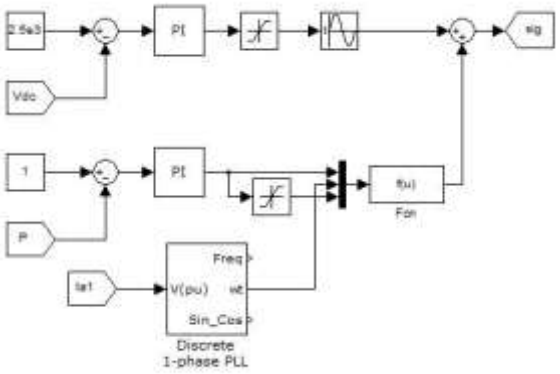


Figure12. Power flow control with voltage phase locked loop (With PI controller)

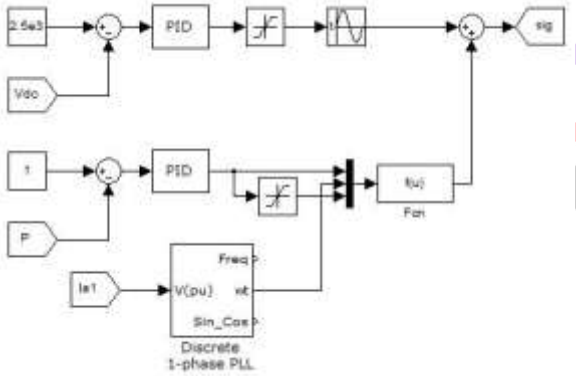


Figure13. Power flow control with voltage phase locked loop (With PID controller).

Note that the feeder voltage unlike the feeder current has no changes during reversal of power flow and becomes a good choice for synchronization. The same control strategy like Fig.12 with current PLL is achievable while it is suitable for one direction power flow demanding. In this strategy the DC bus voltage is more than the difference voltages between feedersat connection points when the power flow is reversed. Also using the voltage phase, there is no need to change the control strategy while power flow is reversed.Fig.11.but Fig 13 is VPLL with PID is good compared to old VPLL PID controller.

V.SIMULATION RESULTS

[1]CURRENT PLL PI CONTROLLERANDCURRENT PLL PID CONTROLLER RESULT ARE COMPARED.

(A) CURRENT PLL WITH PI CONTROLLER OUTPUT WAVEFORM OF POWER, Vdc AND CURRENT.

Fig.14From 0 to 0.5 Sec interval powers is zero after 0.5 to 3 Sec interval power is 1 Pu. Here using the controller is PI. by use of PI controller transient minimum to maximum from 0 to 11 Pu. After the From 3 to 5 Sec intervals the power flow goes to the negative direction but the voltage is increased and current goes to the zero. So, the power flow in 3 to 5 Sec interval is zero. The DC link voltage is maintain 250V at 0 to3 Sec interval, after it's goes to decreased up to 110V.

[B] CURRENT PLL WITH PID CONTROLLEROUTPUT WAVEFORM OF POWER, Vdc AND LINE CURRENT

Fig 15 from 0 to 0.5 Sec interval powers is zero after 0.5 to 3Sec interval power is 1Pu. Here using the controller is PI. By use of PI controller transient min to max is 0 to 7. After the 3 to 5 Sec interval the power flow goes to the negative direction but the voltage is increased and current goes to the zero. So, the power flow in 3 to 5 Sec interval is zero. Compare to PI and PID controller, the transient minimization is better for PID. So the transient stability will improved by using the PID controller. The DC link voltage is maintain 250V at 0 to3 Sec interval, after it's goes to decreased up to 100V.At the point 0 to 3 Sec interval magnitude of the current is 1 after it's goes to zero because of reverse power flow .

[2] VOLTAGEPLL PICONTROLLER AND VOLTAGE PLL PID CONTROLLER RESULT ARE COMPARED

[B] VOLTAGE PLL WITH PI CONTROLLER OUTPUT WAVEFORM OF POWER, Vdc AND LINE CURRENT

Fig 16. From 0 to 0.5 Sec interval power is have some oscillations. After 0.5 to 3 Sec interval power is 0.5 Pu. Here using the controller is PI. After the 3 to 5 Sec interval the power flow goes to the negative direction but the power voltage is decreased and current goes to increasing. So, the flow in 3 to 5 Sec interval is negative 0.5The DC link voltage is Maintain 150V at 0 to 3 Sec interval, after its goes to increased up to 50V.From 0 to 3 Sec interval magnitude of the current is 0.5 after it's increasing because of reverse power flow.

[B] VOLTAGE PLL WITH PID CONTROLLEROUTPUT WAVEFORM OF POWER, Vdc AND LINE CURRENT

Fig 17. At 0 to 3 Sec interval power is 0.5 Pu. Here using the controller is PID after the 3 to 5 sec interval the power flow goes to the negative direction but the voltage is decreased and current goes to increasing. So, the power flow in 3 to 5 Sec interval is negative 0.5.Compare to PI and PID controller, the transient minimization is better for PID. So the transient stability will improved by using the PID controller. The DC link voltage is maintain 150V at 0 to3 Sec interval, after it's goes to increased up to 50V.At the point 0 to 3 Sec interval magnitude of the current is 0.5 after it's increasing because of reverse power flow.

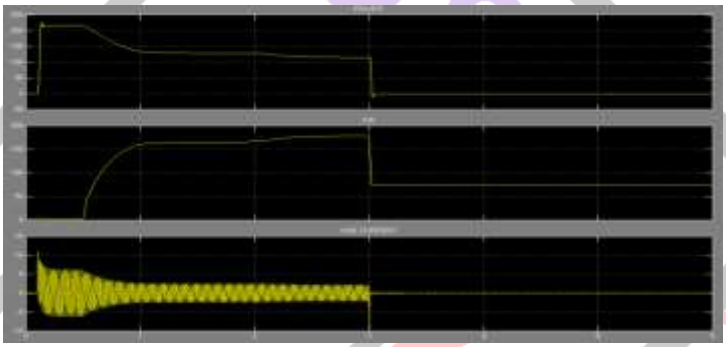


Fig: 14 power Vdc and line current

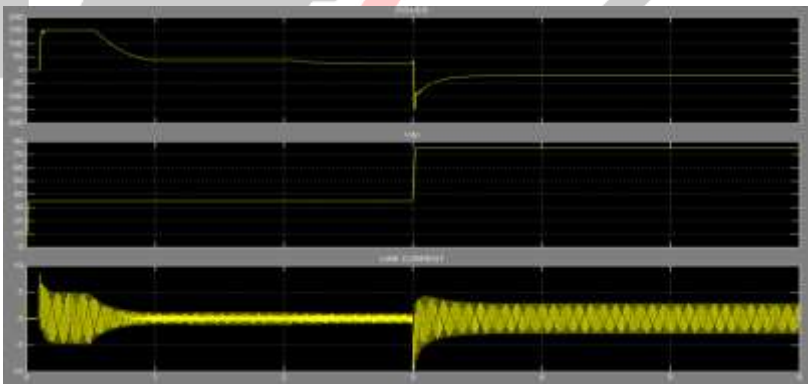


Fig: 15 power Vdc and line current

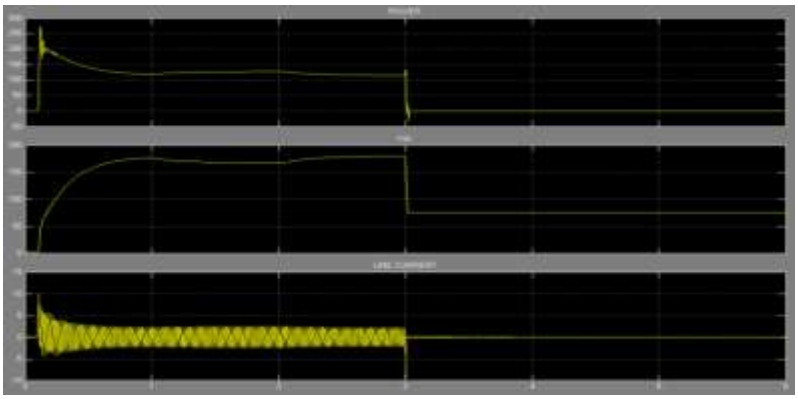


Fig: 16 power, Vdcand line current

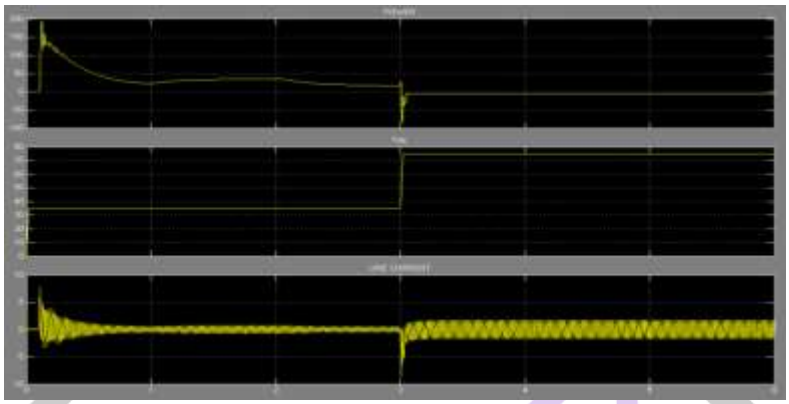


Fig: 17 power Vdc and line current.

COMPARISON OF **THD** FOR **PI** AND **PID** CONTROLLER FOR BOTH CASES

S.NO	CONTROLLER	PLL	THD (%)
1	PI	CURRENT	26.52
2	PI	VOLTAGE	26.38
3	PID	CURRENT	25.20
4	PID	VOLTAGE	24.63

VI. CONCLUSION

The entire study about DSSSC is done using MATLAB software. Distributed Static Series Synchronous Compensator (DSSSC) is modeled for a distribution system that handles power reversal. The power reversal without DSSSC is distorted, power flow is improper and real and reactive powers are unstable. So a control strategy with current phase locked loop and voltage phase locked loop to control the overall system is analyzed using PI and PID controller for transient performance and positive results are obtained. With DSSSC compensator the power reversal is possible. The PI controller eliminates the offset at the expense of maximum overshoot and more settling time. With PID controller there is reduced maximum overshoot and the system achieves the steady state with less settling time. Thus PID is the ultimate process composite controller.

The total harmonic distortion (THD) for the system with compensation (VPLL, PI controller) is 26.38%and proposed compensation (VPLL, PID controller) is 24.63%. From this, we can clearly state that the THD for the system with compensation reduces the harmonics

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