Design of Modified Low Power and High Speed Carry Select Adder Using Brent Kung Adder

[1]Amala Maria Alex, [2]Nidhish Antony

[1]MTech in VLSI & Embedded Systems, [2]Assistant Professor ECE Dept
Mangalam college of Engineering, Kottayam, Kerala, India

Abstract—In order to perform the addition of two numbers adder is used. Adder also forms the integral part of ALU. Besides this application of adder in computer, it is also employed to calculate address and indices and also operation codes. Different algorithm in Digital Signal Processing such as FIR and IIR are also employed using adder. What all matter is speed and so it is the most important constraint. The important areas of VLSI areas are low power, high speed and data logic design. In Carry Select adder the possible value of input carry are 0 and 1. So in advance, the result can be calculated. Further we have the multiplexer stage, for calculating the result in its advanced stage. The conventional design is the use of dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA (Cin=0) is replaced by Brent kung adder. As, RCA (for Cin=1) and Brent Kung adder (for Cin=0) consume more chip area, so an add-one scheme i.e., Binary to Excess-1 converter is introduced. Also the square root adder architectures of CSA are designed using Brent Kung adder in order to reduce the power and delay of adder. In proposed model a modification is done by using D-LATCH instead of Binary to Excess-1 to improve the speed and reduce power. Here the Binary to Excess-1 Converter is replaced with a D-Latch. Initially when en=1, the output of the BK adder is fed as input to the D-Latch and the output of the D-latch follows the input and given as an input to the multiplexer. When en=0, the last state of the D input is trapped and held in the latch and therefore the output from the BK adder is directly given as an input to the Mux without any delay.

Index Terms— BK Adder-Brent Kung Adder,RCA-Ripple Carry Adder,CSLA-Carry Select Adder,RLBKCSLA-Regular Linear Brent Kung Carry Select Adder,MLBKCSLA-Modified Linear Brent Kung Carry Select Adder,RSQBKCSLA-Regular Square Root Brent Kung Carry Select Adder,MSQBKCSLA-Modified Square Root Brent Kung Carry Select Adder,PSQBKCSLA-Proposed Square Root Brent Kung Carry Select Adder

I. INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. Adders are used in multipliers, in DSP to execute various algorithms like FFT, FIR and IlR. Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important constraint. Design of low power, high speed data path logic systems are one of the most essential areas of research in VLSI. In CSA, all possible values of the input carry i.e. 0 and 1 are defined and the result is evaluated in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. Conventional Carry Select Adder is designed using dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA (Cin=l) is replaced by Brent kung adder[3].

As, RCA (for Cin=O) and Brent Kung adder (for Cin=l) consume more chip area, so an add-one scheme i. e. , Binary to Excess-l converter is introduced. Also the square root adder architectures of CSA are designed using Brent kung adder in order to reduce the power and delay of adder. In this paper, Modified Square Root Carry select Adder using Brent Kung adder is proposed using single BK and BEC instead of dual RCAs in order to reduce the power consumption with small penalty in speed.

II. LITERATURE REVIEW

In Electronics, carry-select adder is a particular way to implement an adder. It is a logic element that computes the sum of two n-bit numbers. The carry-select adder generally composes of two ripple carry adders and a multiplexer.

Ripple Carry Adder

The Ripple Carry Adder is used to compute addition of two N-bit numbers. It consists of N full adders to add N-bit numbers. From the second full adder, carry input of every full adder is the carry output of its previous full adder. This kind of adder is typically known as Ripple Carry Adder because carry ripples to next full adder. The layout of Ripple Carry Adder is simple, which allows fast design time. The Ripple Carry Adder is slowest among all the adders because every full adder must wait till the previous full adder generates the carry bit for its input. The 3-bit RCA is shown in Fig 1. Theoretically the Ripple Carry Adder has delay of $o(n)$ and area of $o(n)$ [6].
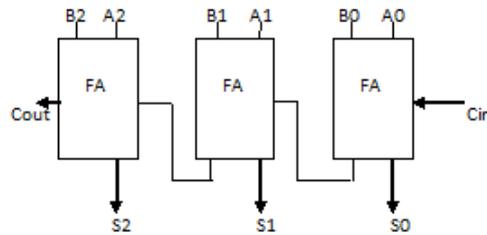
Fig. 1: 3-bit Ripple Carry Adder [3]

Multiplexer

Multiplexer is a combinational circuit which has many inputs and single output. Depending on the select input combination the content on one of the selected input line is transferred on to the output line. It is also widely known as many to one circuit, data selector and universal parallel to serial converter. The 6:3 Multiplexer is shown in Fig.2[6].
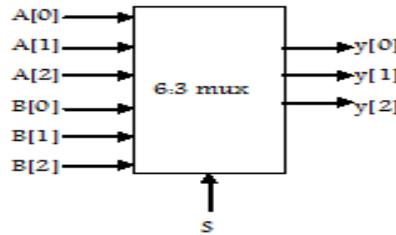

Fig. 2. 6:3 multiplexer [3]

Carry Select Adders

The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known[6].
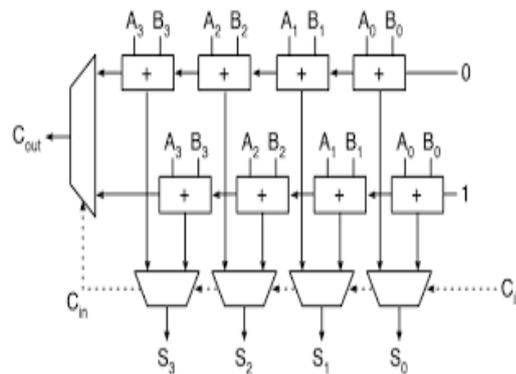

Fig.3:Carry select adder[6]

The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs for a block size of $\sqrt{n}$ When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The o$\sqrt{n}$ delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

III.EXISTING WORKS

Parallel Prefix Adder

The parallel prefix adders are more flexible and are used to speed up the binary additions. Parallel prefix adders are obtained from Carry Look Ahead (CLA) structure. We use tree structure form to increase the speed of arithmetic operation. Parallel prefix adders are fastest adders and these are used for high performance arithmetic circuits in industries. The construction of parallel prefix adder involves three stages [1].
1. Pre- processing stage
2. Carry generation network
3. Post processing

Pre-Processing Stage

In this stage we compute, generate and propagate signals toeach pair of inputs A and B. These signals are given by the logic equations 1&2:

$$P_i = A_i \ XOR \ B_i \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(1)$$
$$G_i = A_i \ AND \ B_i \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(2)$$

Carry Generation Stage

In this stage we compute carries corresponding to each bit. Execution of these operations is carried out in parallel. After the computation of carries in parallel they are segmented into smaller pieces. It uses carry propagate and generate as intermediate signals which are given by the logic equations 3&4:

$$CP_{i:j} = P_{i:k+1} \ and \ P_{k:j} \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(3)$$
$$CG_{i:j} = G_{i:k+1} \ or(P_{i:k+1} \ and \ G_{k:j}) \dots\dots\dots\dots\dots(4)$$

The operations involved in fig. 1 are given as:
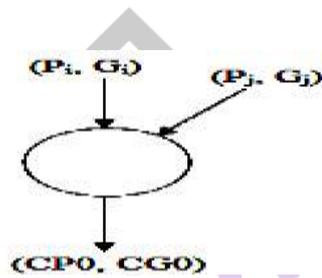CPO=Pi and Pj
CGO=(Pi and Gj) or Gi

Fig.4: Carry network [1]

Post Processing Stage

This is the concluding step to compute the summation of input bits. It is common for all the adders and the sum bits are computed by logic equation 5& 6:

$$C_{i-1} = (P_i \ and \ C_{in}) \ or \ G_i \qquad (5)$$
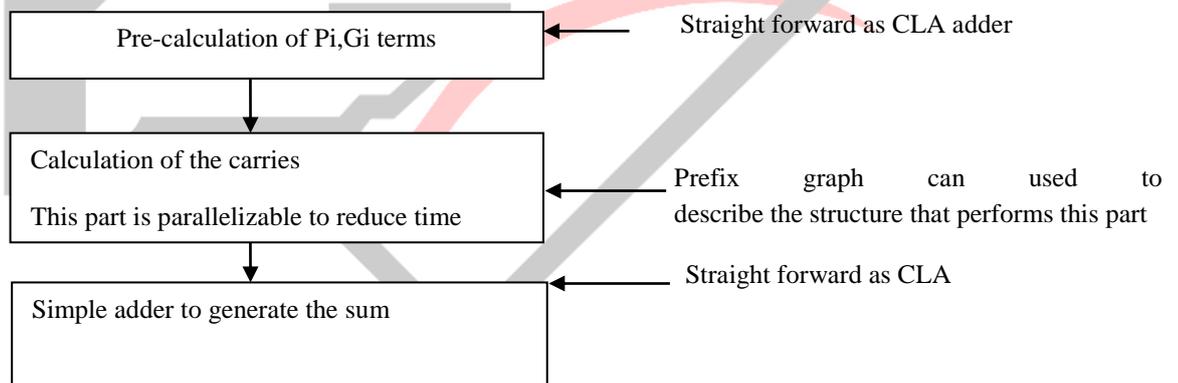$$S_i = P_i \ xor \ C_{i-1} \qquad (6)$$

Fig 5:.Different stages of carry tree adders[3]

Brent Kung Adder

Brent-Kung adder is a very popular and widely used adder. It actually gives an excellent number of stages from input to all outputs but with asymmetric loading of Intermediate stages. It is one of the parallel prefix adders. It is one of the parallel prefix adders where these adders are the ultimate class of adders that are based on the use of generate and propagate signals. In case of Brent kung adders along with the cost, the wiring complexity is also less. But the gate level depth of Brent-Kung adders is 0 (log2 (n)), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Fig.6[1][2].
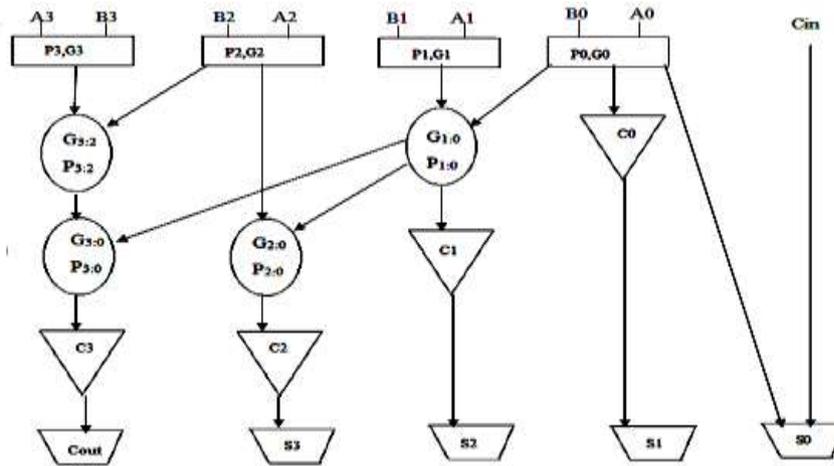
Fig. 6: 4 –bit Brent Kung Adder [1]

IV.REGULAR LINEAR BRENT KUNG CARRY SELECT ADDER

Conventional Carry Select Adder consists of dual Ripple Carry Adders and a multiplexer. Brent Kung Adder has reduced delay as compared to Ripple Carry Adder. So, Regular Linear BK CSA is designed using Brent Kung Adder. Regular Linear BK CSA consists of a single Brent Kung adder for Cin=O and a Ripple Carry Adder for Cin=1. It has four groups of same size. Each group consists of single Brent Kung adder, single RCA and multiplexer. We use tree structure form in Brent Kung adder to increase the speed of arithmetic operation. The block diagram of Regular Linear BK CSA is shown in Fig. 7[1][2].
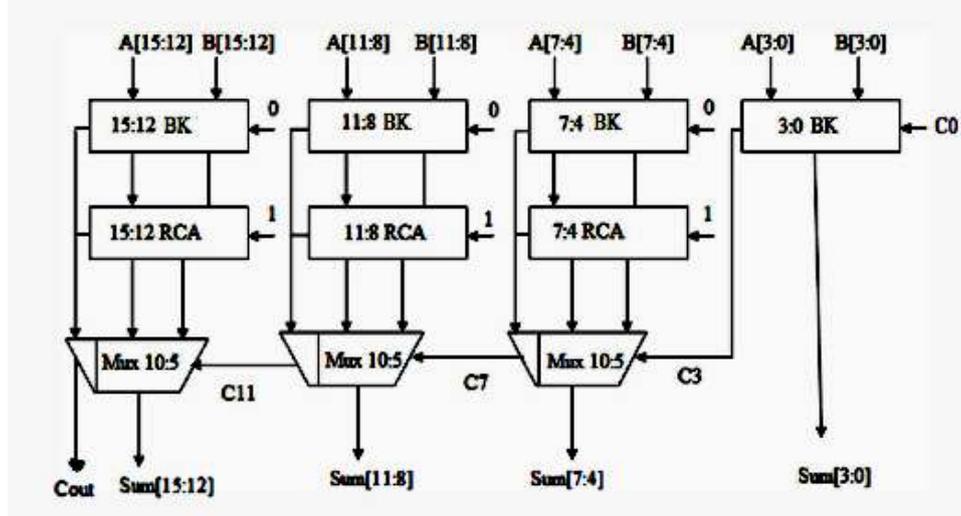

Fig.7: Block Diagram of 16-bit Regular Linear BK Carry Select Adder [1]

In group 2 of Regular Linear CSA, there are single BK for Cin=O and single RCA for Cin=1. Now, the C3 tells whether the input carry is 0 or 1 and depending on its value the output of particular block is selected. If C3=0 then the output of BK with Cin=O is selected using 10:5 multiplexer and if C3=1 then output of RCA with Cin=l is selected using the MUX. A 4-bit   Sum [7:4] and an output carry, C7 is obtained at the output of group 2.

V.MODIFIED LINEAR BRENT KUNG CARRY SELECT ADDER

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin=1 and Brent Kung adder for Cin=0 and so it consumes more area. To solve this problem add-one schemes like Binary to Excess- 1 Converter (BEC) have been introduced. Using BEC, Regular Linear BK CSA is modified in order to obtain a reduced area and power consumption. Binary to Excess-l converter is used to add 1 to the input numbers. So, here ripple carry adder with Cin=1 will be replaced by BEC because it require less number of logic gates for its implementation so the area of circuit is less. A circuit of 4-bit BEC and truth table is shown in Figure 8 and table 1[1][3].
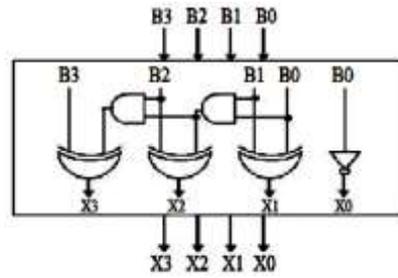
Fig.8: 4-bit Binary to Excess-I code Converter [1]

The Boolean expressions of 4-bit BEC are listed below,
(Note: functional symbols, - NOT, & AND, /\ XOR).

$$X0 = -B0$$
$$X1 = B0(1)/\backslash B1$$
$$X2 = B2 /\backslash (B0\ \&\ B1)$$
$$X3 = B3 /\backslash (B0\ \&\ B1\ \&\ B2)$$

Binary Logic B₀ B₁ B₂ B₃	Excess-1 Logic X₀ X₁ X₂ X₃
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

Table I. Truth table of 4-BIT Binary to Excess-I converter[1]

Linear Modified BK CSA is designed using Brent Kung adder for Cin=O and Binary to Excess-l Converter for Cin=l in order to reduce the area and power consumption with small speed penalty. Linear Modified BK CSA consists of 4 groups. Each group consists of single BK adder, BEC and multiplexer. The block diagram of Linear Modified BK CSA is shown in fig.9[1].
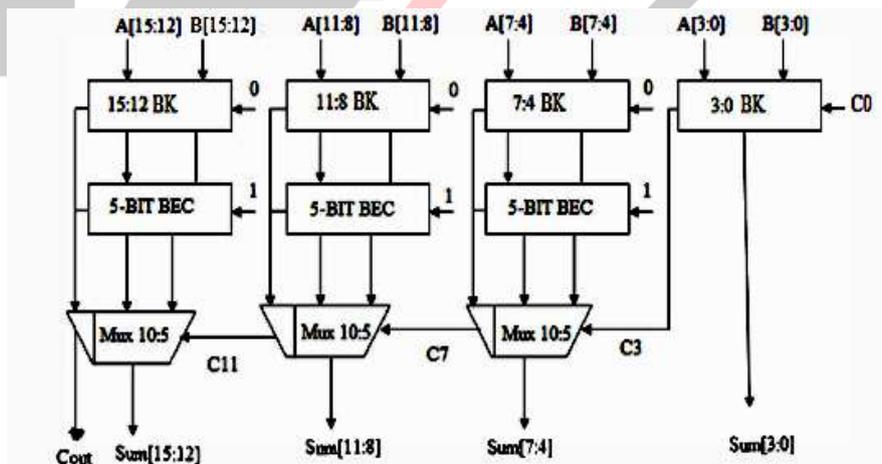

Fig.9: Block Diagram of 16-bit Linear Modified BK Carry Select Adder [1]

To replace the N-bit Brent Kung adder, a N+l bit BEC is required. The importance of BEC logic comes from the large silicon area reduction when designing Linear Modified BKCSA for large number of bits. The N bit Brent Kung adder perform the addition operation corresponding to Cin=0 and Binary to Excess logic perform the addition operation corresponding to Cin=1. The real value of Cin that is C3 for group 2, will help the multiplexer to choose either sum corresponding to Cin=0 or Cin=1[1].

VI.REGULAR SQUARE ROOT BRENT KUNG CARRY SELECT   ADDER

Regular Linear Brent Kung Carry Select Adder consumes large area and to reduce its area a new design of adder is used i.e. Regular Square Root Brent Kung Carry Select Adder. Regular Square Root BK CSA has 5 groups of different size Brent Kung adder. Each group contains single BK for Cin=O, RCA for Cin=1 and MUX. The block diagram of the 16-bit regular SQRT BK CSA is shown in Fig. 10. High area usage and high time delay are the two main disadvantages of Linear Carry Select Adder. These disadvantages of linear carry select adder can be rectified by SQRT CSA. It is an improved version of linear CSA. The time delay of the linear adder can decrease, by having one more input into each set of adders than in the previous set. This is called a Square Root Carry Select Adder. There are 5 groups in Regular Square Root BK Carry Select Adder. Here single Brent Kung adder is used for Cin=O and ripple carry adder is used for Cin=l and then there is a multiplexer stage. Due to the presence of RCA and BK, this circuit consumes large area[1].
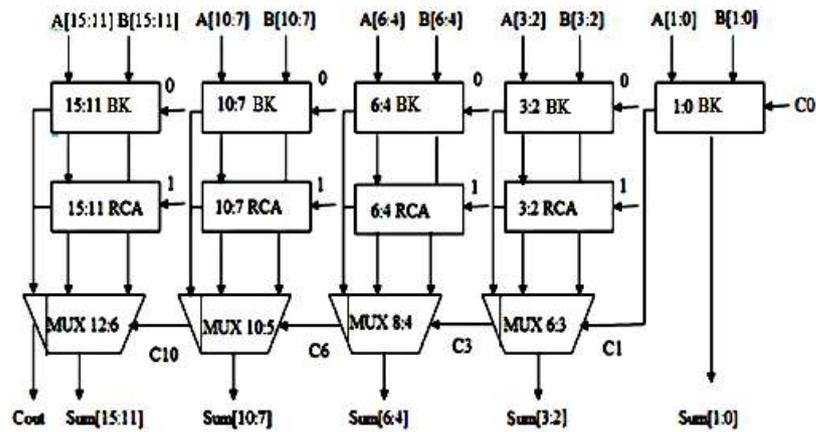

Fig. 10: Block Diagram of l6-bit Regular Square Root BK Carry Select Adder [1]

VI. MODIFIED SQUARE ROOT BRENT KUNG CARRY SELECT ADDER

Modified Square Root Brent Kung Carry Select Adder has been designed using Brent kung adder for Cin=O and BEC for Cin=l and then there is a multiplexer stage. It has 5 groups of different size Brent Kung adder and Binary to Excess-l Converter (BEC). BEC is used to add 1 to the input numbers. Less number of logic gates are used to design BEC as compared to RCA therefore it consumes less area. The block diagram of the 16-bit modified Square Root BK Carry Select Adder is shown in Fig. 11. Each group contains one BK, one BEC and MUX. For N- Bit Brent Kung adder, N+ 1 Bit BEC is used. Power consumption and delay of this adder is calculated for 16-Bit word size [1].
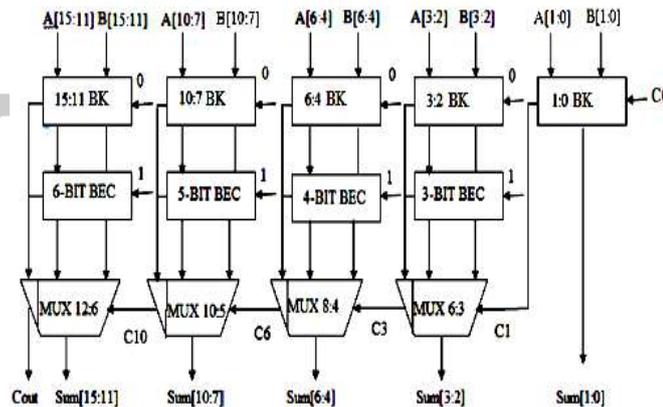

Fig. 11: Block Diagram of 16-bit Modified SQRT BK CSA [1]

VII. PROPOSED SQUARE ROOT BRENT KUNG CARRY SELECT ADDER USING D-LATCH

When the Modified SQRT BK CSA is simulated and synthesized, the area and power is less in the modified CSLA but the delay is slightly increased. So we can improve the above structure in terms of less delay and higher speed by replacing the BEC with a D-Latch. Thus an improved Carry Select Adder with D-Latch is shown in fig.12. Here the Binary to Excess-1 Converter is replaced with a D-Latch. Initially when en=1, the output of the BK adder is fed as input to the D-Latch and the output of the D-latch follows the input and given as an input to the multiplexer. When en=0, the last state of the D input is trapped and held in the latch and therefore the output from the BK adder is directly given as an input to the mux without any delay. Now the mux selects the sum bit according to the input carry which is the selection bit and the inputs of the mux are the outputs obtained when en=1 and 0.
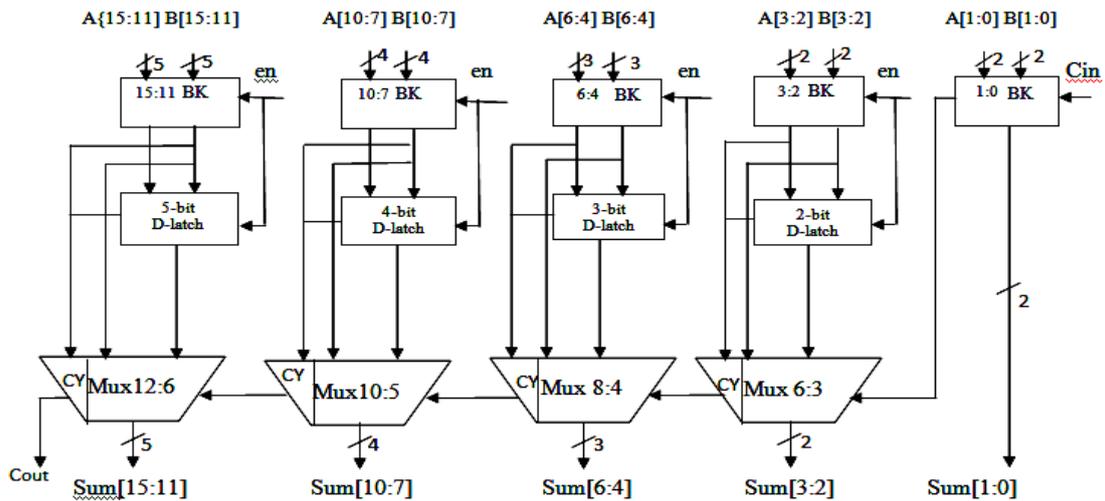
Fig 12.Proposed square root brent kung carry select adder

D-Latch

Latch is an electronic device that can be used to store one bit of information. The D latch is used to capture, or 'latch' the logic level which is present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch. Fig. 12 shows the logic diagram of D-Latch [6] .
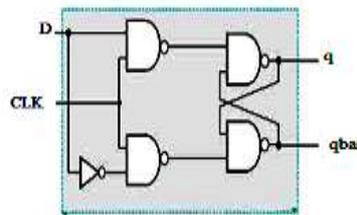

Fig. 12: D-latch[4]

Working Of Proposed Square Root Brent Kung Carry Select Adder

Here initially when en=1, the output of the BK adder is fed as input to the D-Latch and the output of the D latch follows the input and given as an input to the multiplexer. When en=0, the last state of the D input is trapped and held in the Latch and therefore the output from the RCA is directly given as an input to the mux without any delay. Now the mux selects the sum bit according to the input carry which is the selection bit and the inputs of the mux are the outputs obtained when en=1 and 0.

VIII. IMPLEMENTATION AND RESULTS

Simulation is carried out using Xilinx simulation tool and Spartan 3 as the target device. The major disadvantage of Modified BKCSLAs and Regular BKCSLAs is the increasing delay and power. This disadvantage is overcome in proposed architecture which reduces the delay and power than the regular and modified BKCSLAs. While comparing all these multiplier we can realize that Proposed Square Root Brent Kung Carry Select Adder (PSQBKCSLA) is more efficient in all aspects. Brent kung adder is one of the fastest adders, using this in the CSLA eventually increase the speed of addition process and using D-latch will decrease the power consumption. The result analysis shows that Proposed square Root Brent Kung Carry Select Adder shows better results than the Ripple carry adder architectures in terms transient analysis of delay and power with little increase in delay.

Fig. 13: Simulation result of Proposed Model

TABLE.1

RESULT ANALYSIS OF DIFFERENT CSLAs

Sl.No	CSLA TYPE	DELAY (ns)	POWER (mW)	AREA(No of slices)
1	RLBKCSLA	24.684	212	30
2	MLBKCSLA	19.26	195	27
3	RSQBKCSLA	25.084	182	29
4	MSQBKCSLA	23.212	172	27
5	PSQBKCSLA	17.964	55	30

Delay ,area and power of various adders are listed in table.1.From its evaluation we analyse which adder is better. Power delay product and area delay product is listed in table.2

TABLE.2

PDP AND ADP OF DIFFERENT CSLAs

SL.No	CSLA TYPE	POWER DELAY PRODUCT	AREA DELAY PRODUCT
1	RLBKCSLA	5233.008	740.52
2	MLBKCSLA	3755.7	520.02
3	RSQBKCSLA	4565.288	727.436
4	MSQBKCSLA	3992.464	626.724
5	PSQBKCSLA	988.02	538.92

PDP of PSQBKCSLA is the least as compared to all other CSLA.It is power efficient and having higher speed. This architecture can be used to implement 32 bit,64 bit and higher bit CSLAs.
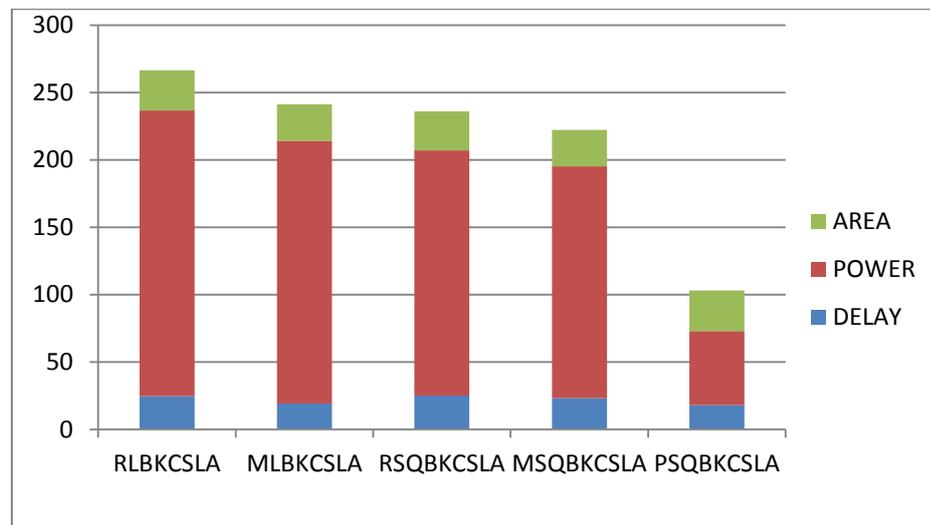
Fig.21: Graphical representation of Area, Power, Delay of CSLAs

From the graphical representation shown in the fig.21 we can easily conclude that PSQBKCSLA have less power and delay. So these adders can be used in multipliers, in DSP to execute various algorithms like FFT, FIR and IIR with ease.

IX CONCLUSION

Power, Delay and Area are the three constituent factors in the VLSI design that limits the performance of the circuit. This work proposes a simple technique to reduce the area and delay In this work, a Proposed Square Root BK Carry Select Adder is proposed which is designed using single Brent kung adder and D-latch instead of using single Brent kung adder for Cin=O and BEC for Cin=l in order to reduce the delay and power consumption of the circuit. Here, the adder architectures like Regular Linear BK CSA, Modified Linear BK CSA, Regular SQRT BK CSA, Modified SQRT BK CSA, Proposed SQRT BK CSA are designed for 16-Bit word size only. This work can be extended for higher number of bits also. By using parallel prefix adder, delay and power consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore Brent kung adder is used. The synthesized results show that power consumption of Proposed SQRT BK CSA is reduced in comparison to other SQRT CSA. So these adders can be used in multipliers, in DSP to execute various algorithms like FFT, FIR and IlR with ease.

REFERENCES

[1] Pallavi Saxena," *Design of Low Power and High Speed Carry SelectAdder Using Brent Kung Adder*" 2015 International Conference on VLSI Systems, Architecture, Technology and Applications (VLSI-SATA)

[2]Pappu P. Potdukhe, Vishal D. Jaiswal *"Review of Carry Select Adder by using Brent Kung Adder"*, 2nd National Conference on Information and Communication Technology (NCICT) 2011 Proceedings published in International Journal of Computer Applications® (IJCA),pp.5-8.

[3] P.Prashanti, Dr. B.Rajendra Naik," *Design and Implementation of High Speed Carry Select Adder*"; International Journal of Engineering Trends and Technology (IJETT) – Volume 4 Issue 9- Sep 2013

[4] Shivani Parmar and Kirat Pal Singh," *Design of High Speed Hybrid Carry Select Adder*", IEEE's 3rd International Advance Computing Conference (IACC) Ghaziabad, ISBN: 978-1-4673-4527-9,22-23 February 2013.

[5] Yajaun He, Chip-Hong Chang, and Jiangmin Gu, "*An area efficient 64Bit square Root carry-select adder for low power Applications*, " in Proc.IEEE International Symposium Circuits and Systems, vol. 4, pp. 40824085,2005.

[6]www.wikipedia.com