A Survey on Gray Code Counting Sequences using Reversible Logic

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***Abstract*—Counting sequences have many applications in logic-circuits. Sometimes it is desirable to have a counting sequence such that the number of bit changes from one codeword to its successor is as large as possible. In any number base there is a plurality of ways that numbers can be encoded. One of the ways for encoding binary is called Gray Code (also known as reflected binary code). An *n*-bit Gray code is a circular listing of the 2^n *n*-bit strings so that successive strings differ only in one bit position. Gray sequence is a counter sequence where the Hamming distance between successive states is one. There are different types of gray code sequences: Binary reflected, Uniformly balanced, Antipodal, Maximum Crossover Hamming Distance, Maximum Gap and Non Composite to name a few. On the other hand Reversible logic has received great attention due to their ability to reduce the power dissipation--an important aspect of low power circuit design. This paper proposes the design of various gray code counters using reversible logic gates and compares their performance.**

***IndexTerms*—Gray Code, Reversible Logic, Hamming Distance, Binary Reflected Gray Code, MCHD, UBGC**

I. INTRODUCTION

One of the major goals in modern circuit design is reduction of power consumption. Bennet proposed that power not to be dissipated if circuit is implemented using reversible gates. This solution promises the arbitrary small fraction of signal energy to be dissipated. Hence reversible logic circuit is getting attention of the researchers in many emerging fields such as nanotechnology, optical computing, and low power CMOS design.

Binary Gray codes which constitute a special type of counting sequences is a well known topic. Although this type of code has been named after its inventor Frank Gray from Bell Laboratories, the code itself actually was demonstrated already by the French engineer ´Emile Baudot in 1878 in a telegraph device. Among all kinds of Gray codes, the binary reflected Gray code, also known as the standard Gray code, is the best known. The usefulness of the binary reflected Gray code and its widespread appearance are undisputed, for instance in algebraic coding theory in the design of combinatorial algorithms, while its optimality with respect to various applications has proved itself frequently. For certain applications however, sometimes additional properties of Gray codes are requested. For instance, when designing experiments, or when designing and testing electrical circuits and information systems. Reversible are circuits (gates) that have one to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states.

Reversible circuits are those circuits that do not lose information. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit. The reversible logic operations do not erase (lose) information and dissipate very less heat. Synthesis of reversible logic circuit differs from the combinational one in many ways. Firstly, in reversible circuit there should be no fan-out, that is, each output will be used only once. Secondly for each input pattern there should be unique output pattern. Finally, the resulting circuit must be acyclic. Any reversible circuit design includes only the gates that are the number of gates, quantum cost and the number of garbage outputs.

II. BASIC DEFINITIONS OF REVERSIBLE LOGIC GATES

Reversible are circuits (gates) that have one to-one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. The Reversible Logic is n-input and k-output Boolean function f(x1, x2, x3… xn) (referred to as (n, k) function) is called reversible if: 1) the number of outputs is equal to the number of inputs 2) each input pattern maps to unique output patterns.

The terminology pertaining to the Reversible Logic Gates is contained in the terms explained below:

1. **Reversible Logic**

   It is an n-Input and n-Output logic function, which has One-to-One Mapping between the inputs and the outputs. Because of this One-to-One Mapping Technique, the output vector can be uniquely determined from the input vector.

2. **Quantum Cost**

   The Quantum Cost refers to the cost of the circuit in terms of the cost of the primitive gates. It is calculated knowing the number of primitive Reversible Logic Gates required for realizing the comparator.

3. Delay

The Delay of a Reversible Logic Gate is the maximum number of gates in a path from any input line to its corresponding output line. The definition of delay is based on the following two assumptions: 1.Each gate performs computation in a unit time. 2. All the inputs fed to the circuit are available before the computation begins.

4. Ancillary Inputs

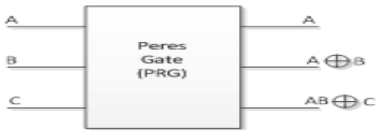
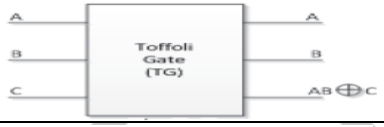
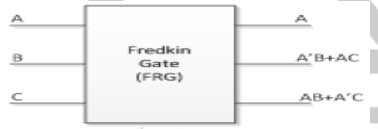
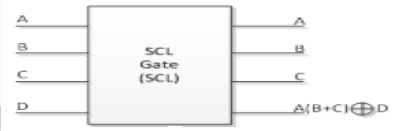
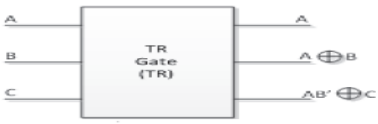
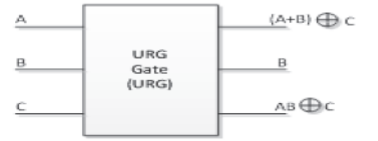
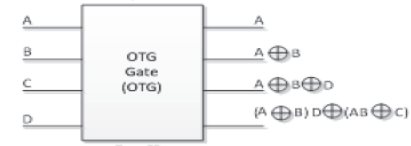
The Ancillary Inputs are defined as the inputs that are to be fed into the Reversible Logic Gates and maintained constant at either "0" or "1". The inputs are to be maintained at a constant value of "0" or "1"in order to synthesize the given logical function.

5. Garbage Outputs

The technique of One-to-One Mapping complies that there must be same number of outputs for the given inputs. The Garbage Outputs are the unutilized outputs in the Reversible Logic Circuits that maintain the reversibility but do not perform any useful operations.

III. Types of Reversible Logic Gates

Table 1 Type of Reversible Logic Gates

Gate	Schematic Representation	Inputs	Outputs
Feynman Gate		A,B	P , Q P = A Q = A⊕ B
Peres Gate		A,B,C	P ,Q , R P = A Q = A⊕B R = AB ⊕C
Toffoli Gate		A,B,C	P ,Q , R P = A Q = B R = AB ⊕C
Fredkin Gate		A,B,C	P ,Q , R P = A Q = $\overline{A}$B ⊕AC R = AB⊕$\overline{A}$C
SCL Gate		A,B,C,D	P,Q,R,S P = A Q =B R = C S = A(B+C)⊕D
TR Gate		A,B,C	P,Q,R P = A Q = A⊕B R = A$\overline{B}$⊕C
New Gate		A,B,C	P,Q,R P = A Q = AB⊕C R = $\overline{A}$ $\overline{C}$ ⊕$\overline{B}$
URG Gate		A,B,C	P,Q,R P = (A+B)⊕C Q = B R = AB⊕C
OTG Gate		A,B,C,D	P,Q,R,S P = A Q = A⊕B R = A⊕B⊕D S= (A⊕B)D⊕(AB⊕C)

IV. Types of Gray Codes

The reflected binary code (RBC), also known as Gray code after Frank Gray, is a binary numeral system where two successive values differ in only one bit (binary digit). The reflected binary code was originally designed to prevent spurious output

from electromechanical switches. Today, Gray codes are widely used to facilitate error correction in digital communications such as digital terrestrial television and some cable TV systems. A Gray code is a code assigning to each of a contiguous set of integers, or to each member of a circular list, a word of symbols such that each two adjacent code words differ by one symbol. These codes are also known as single-distance codes, reflecting the Hamming distance of 1 between adjacent codes.

Binary Reflected Gray Code (BRGC):

It is the most common form of gray code and vastly superior in communications protocols. The sequence is shown in Table 2. But generally this is not the optimal code for use as output for mechanical actuators where it is preferred to have a coding system that provides more uniformity. Two measures of uniformity are the transition counts and the gap of the code.

Antipodal Gray Codes (APGC):

An n-bit Antipodal Gray Codes have the additional property that the binary complement of any code string appears exactly n steps away in the list. Thus the spatial frequency of the antipodal Gray code-pattern is similar along frames. The code is as shown in Table 2.

Uniformly Balanced Gray Code (UBGC):

Gray codes with the interesting property that the number of state transitions per bit is more uniformly distributed among the bit positions. For 4-bit UBGC each bit changes state exactly four times. The sequence of UBGC in the lexicographical order is tabulated in Table 2.

Maximum Crossover Hamming Distance Gray Code (MCHDGC):

Two code words in a Gray code G(n) of length n are said to crossover each other in a cyclic n-bit Gray code if their distance in the list is equal to 2^n -1 . If any two crossover code words in a cyclic n-bit Gray code have the same Hamming distance k and if this Hamming distance is maximal for fixed n, the code is called a Gray code with maximum crossover Hamming distance (MCHD) k.

Table 2 Gray Code Sequences

BRGC	*APGC*	*UBGC*	*MCHDGC*
0000	0000	0000	0000
0001	0001	1000	0001
0011	0011	1100	0011
0010	0111	1101	0010
0110	1111	1111	0110
0111	1110	1110	0100
0101	1100	1010	0101
0100	1000	0010	0111
1100	1010	0110	1111
1101	1011	0100	1110
1111	1001	0101	1100
1110	1101	0111	1101
1010	0101	0011	1001
1011	0100	1011	1011
1001	0110	1001	1010
1000	0010	0001	1000

V. DESIGN OF GRAY CODE COUNTERS

1. *Conventional Gray code Counter:*

Gray codes have the useful property that consecutive numbers differ in only a single bit position. In this paper we design the binary reflected code using conventional logic gates. The counting sequence of this counter is shown in Table 2. The schematic design and output sequences are shown in Figure 1 and Figure 2 respectively.

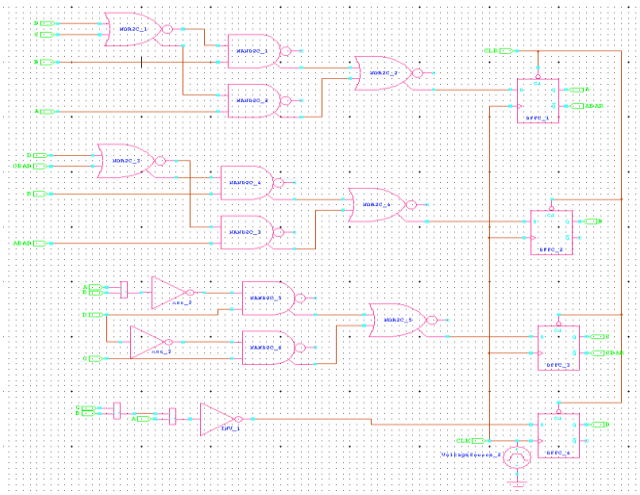


Fig.1 Conventional Gray code Counter

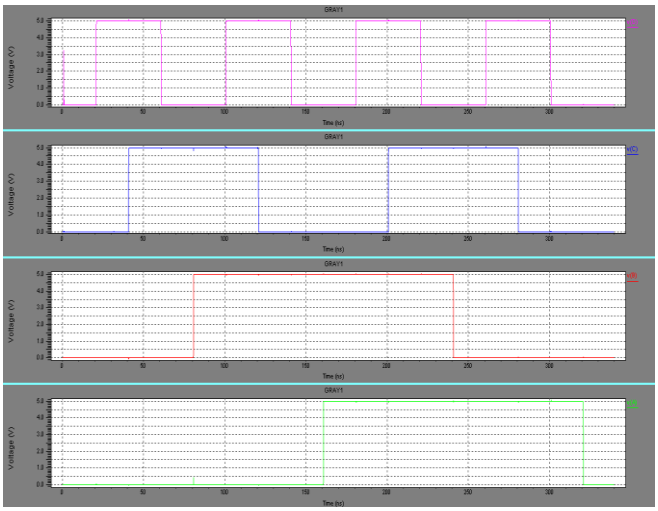


Fig.2 Output of Conventional Gray code Counter

2. ***Binary Reflected Gray Code Counter (BRGCC):***

The binary reflected code counting sequence is given in the Table 2. The design equations are given below. The counting sequence of the BRGCC is shown in Figure 3. The schematic implementation of Binary Reflected Gray Code Counter using reversible logic gates and its output is shown in Figure 4 and Figure 5.

Design Equations:

$$D3 = A(C+D) + B\,\overline{C}\,\overline{D}$$

$$D2 = B\,(\overline{C} + D) + \overline{A}\,C\,\overline{D}$$

$$D1 = (\overline{A \oplus B}\,)\,D + C\,\overline{D}$$

$$D0 = (\,\overline{A \oplus B \oplus C}\,)$$

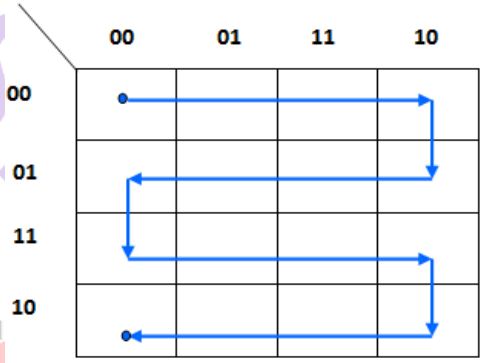


Fig.3 BRGCC Counting Sequence

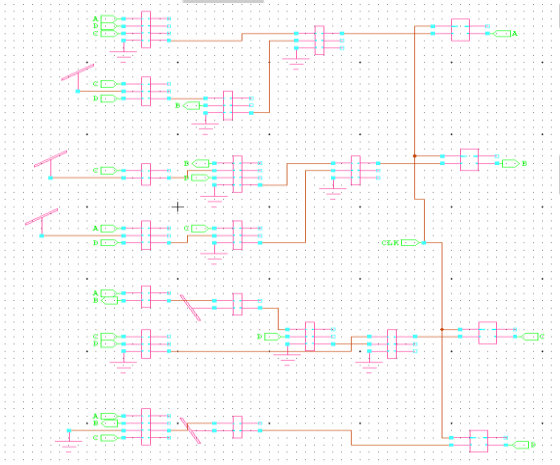


Fig.4 Binary Reflected Gray code Counter

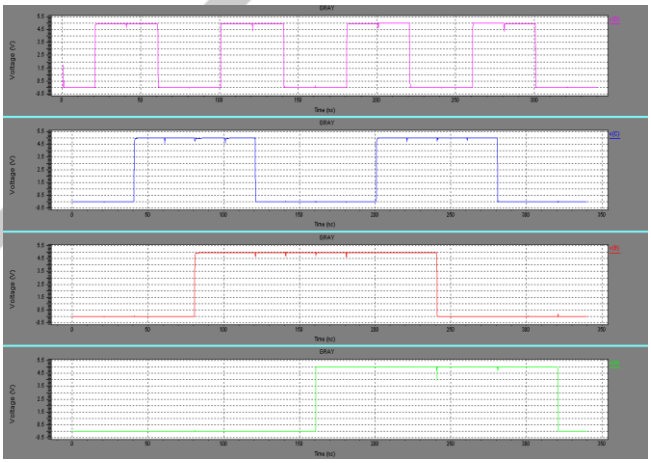


Fig.5 Output of Binary Reflected Gray code Counter

3. ***Antipodal Gray Code Counter (APGCC):***

The Antipodal Gray Code counting sequence is given in the Table 2. The design equations are given below. The counting sequence of the APGCC is shown in Figure 6. The schematic implementation of Antipodal Gray Code Counter using reversible logic gates and its output is shown in Figure 7 and Figure 8.

Design Equations:

$$D3 = A\,(\overline{BD}) + B\,C\,D$$

$$D2 = B\,(\overline{A \oplus C}) + D\,(A \oplus C)$$

$$D1 = \overline{A}\,(B \oplus D) + A\,\overline{B}\,\overline{D} + B\,C\,D$$

$$D0 = \overline{B}\,(\overline{A \oplus C}) + D\,(A \oplus C)$$

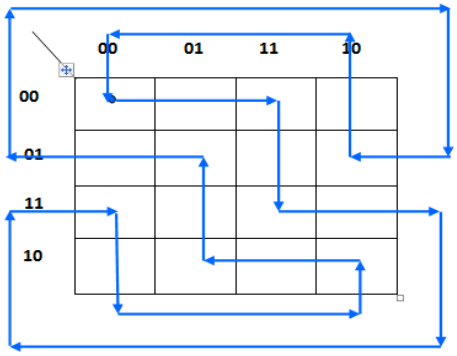


Fig.6 APGCC Counting Sequence

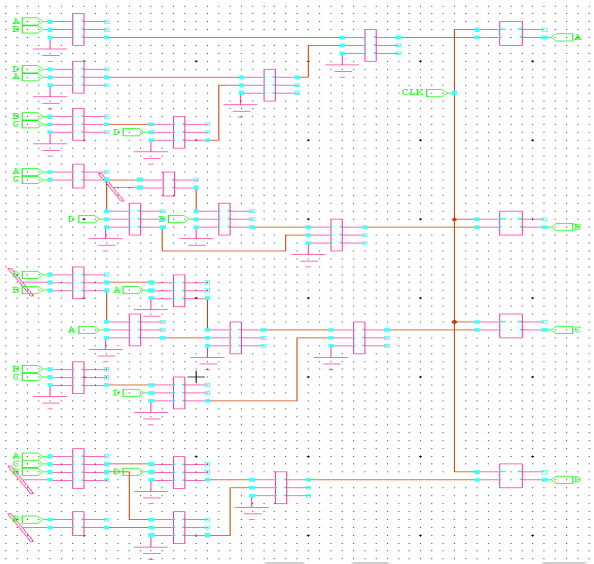


Fig.7 Antipodal Gray code Counter

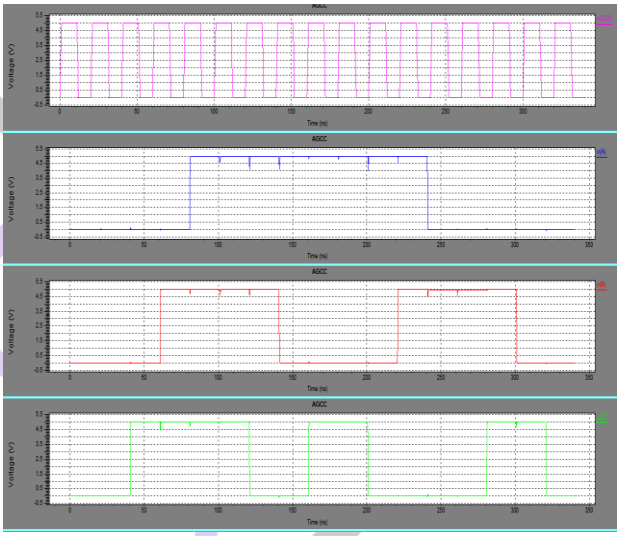


Fig.8 Output of Antipodal Gray code Counter

4. *Uniformly Balanced Gray Code Counter (UBGCC):*

The schematic implementation of Uniformly Balanced Gray Code Counter using reversible logic gates and its output is shown in Figure 9 and Figure 10

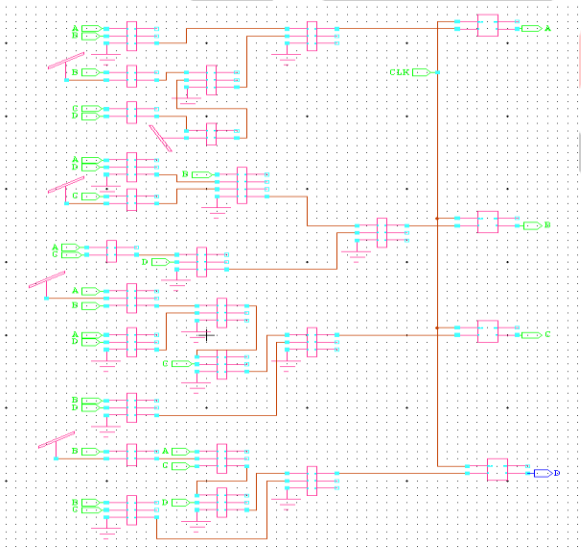


Fig.9 Uniformly Balanced Gray code Counter

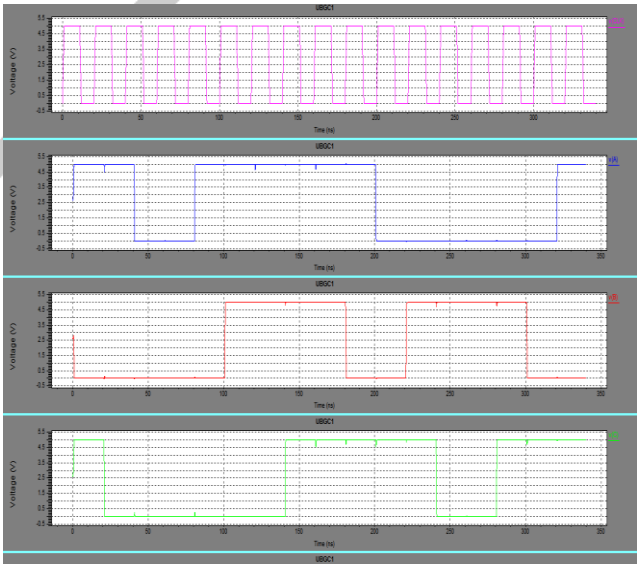


Fig.10 Output of UBGC Counter

5. *Maximum Crossover Hamming Distance Gray Code Counter (MCHDGCC):*

The schematic implementation of Maximum Crossover Hamming Distance Gray Code Counter using reversible logic gates and its output is shown in Figure 11 and Figure 12 .

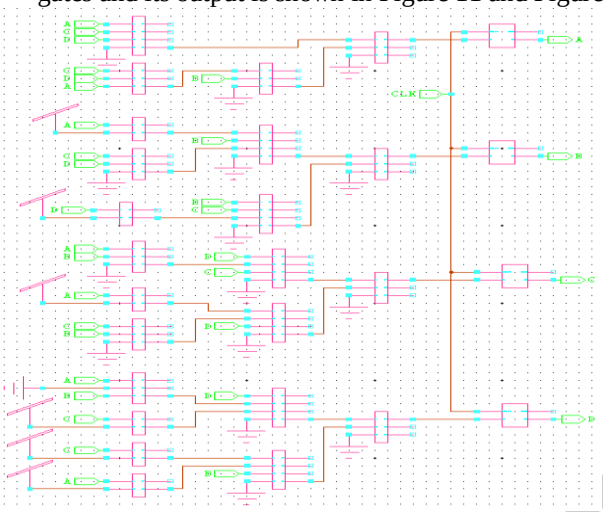


Fig.11 MCHD Gray code Counter

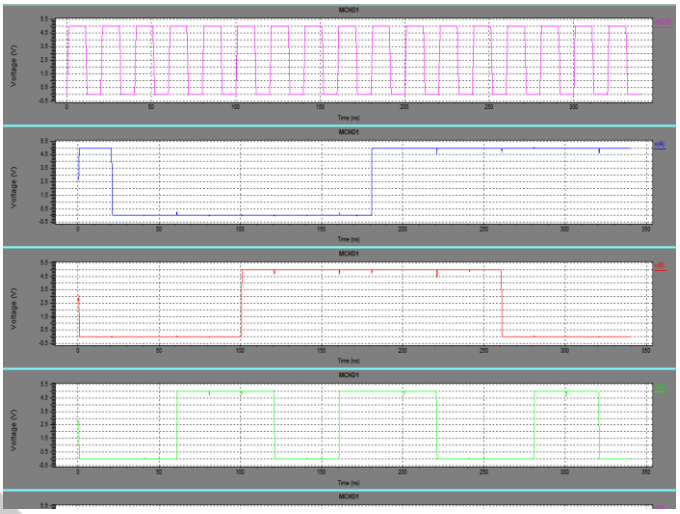


Fig.12 Output of MCHD Gray code Counter

VI. RESULTS

The power consumption of various gray code counters implemented with reversible logic gates are tabulated in Table 3.

Table 3 Power Consumption of various gray code counters

Design	Power Consumption
BRGCC using conventional logic gates	1.311321e-002 watts
BRGCC using reversible logic gates	1.986801e-003 watts
APGCC using reversible logic gates	4.028287e-003 watts
UBGCC using reversible logic gates	3.047122e-003 watts
MCHDGCC using reversible logic gates	2.173780e-003 watts

VII. CONCLUSION

Gray Code counters are unit distance counters since the adjacent words have only one bit change. Gray code counters can be used for asynchronous FIFO's address pointers. They reduce the digital noise as compared to the normal counters. They also find application in data path synchronization. They are widely used to facilitate error correction in digital communication such as digital terrestrial television and some cable TV systems.

This paper gives a comparative study of gray code variants namely Binary reflected code counter, Antipodal gray code counter, uniformly balanced gray code counter and maximum crossover hamming distance gray code counter. These four variants are analyzed in terms of power consumption tabulated in table 3. The counters are simulated and verified using T-Spice and W-edit.

VIII. FUTURE SCOPE

The additional properties of gray code can be used in various practical applications. The paper can further be extended towards the designing other counting sequences like Maximum Gap Gray Code Counter, Non Composite Gray Code etc., Reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. This work forms an important move in building asynchronous FIFO, UART and complex reversible sequential circuits for quantum computers. The future work could be to develop efficient reversible counters and reversible controller circuits.

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