

DESIGN OF SENSORLESS CAPACITOR VOLTAGE BALANCING CONTROL FOR THREE-LEVEL BOOSTING PFC WITH PV SYSTEM

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Abstract – In this paper we compared with the conventional boosting PFC converter, the three-level boosting PFC converter has two cascaded switches and two cascaded capacitors across the dc-side voltage. Two capacitor voltages may be different due to their mismatched equivalent series resistance, their mismatched capacitance, and the mismatched conducting time of the corresponding switches. It follows that the controller needs to sense the capacitor voltages to balance both capacitor voltages. In this paper, the sensor less capacitor voltage balancing control (SCVBC) without sensing the capacitor voltages is proposed, and the total number of the feedback signals is saved. The proposed SCVBC is digitally implemented in an FPGA-based system. The provided simulated and experimental results also demonstrate the proposed SCVBC. The entire system will be performed using PV system also.

I. INTRODUCTION

To reduce the power transmission loss and increase the system stability, more and more power-electronics products are forced to include the power factor correction (PFC) function. Generally speaking, the PFC function includes shaping the ac-side current waveform and regulating the dc-side voltage. Due to the characteristics of the continuous current, the boost-derived PFC converters have been widely used to achieve the desired PFC function. For the conventional boost dc/dc converter, the single switch needs to withstand the dc output voltage when the single switch blocks. Two cascaded switches and two cascaded capacitors are connected together in the three-level boosting dc/dc converter. When one of the switches conducts and the other blocks, the blocking switch needs to withstand only half dc output voltage if both capacitor voltages are balanced. If not balanced, one of the capacitor voltages may be larger than the breakdown voltage of the switch, which would contribute to make damage to the switch. It is noted that the inductor voltage in the three-level boost dc/dc converter has three levels, which makes the three-level boosting dc/dc converter to have smaller inductor current ripple

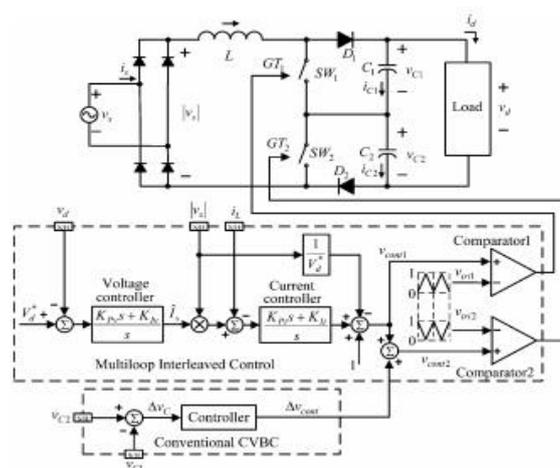


Fig. 1. Three-level boosting PFC converter with multi loop feed forward control and the conventional capacitor voltage balancing control loop than the boost converter under the same switching frequency. Therefore, the three-level boost converters are often used in the high-voltage-ratio applications, such as the fuel cell applications and the grid-connected applications. In addition, the high-withstanding-voltage semiconductor switches often have higher cost and the larger drain-source resistances than the low-withstanding- voltage ones. Thus, the three-level boost converter has the additional advantages of the low switching loss and the high efficiency. The three-level boosting PFC converter was first proposed in by connecting the diode rectifier to the three-level boosting dc/dc converter. In the multi loop interleaved control combining the multi loop control and the interleaved PWM scheme was first proposed to control the three-level boosting PFC converter. The multi loop control includes the feed forward loop, the inner current loop, and the outer voltage loop. The three single-phase three-level boosting PFC

converter in Delta connection is used to achieve the three-phase PFC function with the ability of redundancy. However, the balance between two capacitor voltages should be noted. In practice, the mismatched capacitances and the mismatched equivalent series resistance (ESR) would result in the voltage imbalance. Therefore, the control of the three-level boosting converter needs to balance both capacitor voltages. In the literature, the voltage balancing control loop for three-level boosting converters can be found. In fact, the other voltage balancing control can be found in the controls of the half-bridge PFC converter and the multilevel inverter. All the methods need to sense capacitor voltages to detect the voltage imbalance and yield the desired voltage balancing function. The multi loop interleaved control with conventional capacitor voltage balancing control (CVBC). One control signal is generated by the multi loop control, and the other control signal is yielded by CVBC with sensing the capacitor voltages. For the three-level boosting dc/dc converter, a voltage balancing control method with sensing only inductor current was first proposed in. In this paper, the concept in is extended to the three-level boosting PFC application and the proposed controller is named the sensor less capacitor voltage balancing control (SCVBC). The voltage imbalance between two capacitor voltages is skilfully detected by sensing the inductor current. The detailed analysis and the design rule of the proportion- type voltage balance controller are also provided. It follows that sensing individual capacitor voltage is not required, and at least one voltage sensor is saved. The provided simulation and experimental results show the effectiveness of the proposed SCVBC.

II. LITERATURE SURVEY

The input ac voltage $v_s = \hat{V} \sin(2\pi ft)$ is assumed to be a sinusoidal function with a peak amplitude \hat{V} . Through the diode rectifier, the input voltage of the three-level boosting converter can be expressed with the rectified voltage $|v_s|$. By assuming that the switching frequency f_s is much larger than the line frequency f , the control signals v_{cont1} and v_{cont2} can be regarded as two constants within the switching period $T_s = 1/f_s$. In addition, the ideal inductor and the ideal capacitors are assumed. That is, the inductor resistance and the capacitor resistances are assumed to be zero. In Fig. 1, two triangular signals v_{tri1} and v_{tri2} are interleaved by 180° . The conventional multi loop control generates the control signal v_{cont1} , and then, the gate signal $GT1$ is generated from the comparison of the control signal v_{cont1} and the triangular signal v_{tri1} . After sensing both capacitor voltages, the voltage imbalance is detected and the conventional CVBC generates the compensation signal Δv_{cont} . Then, the other control signal v_{cont2} is obtained by adding the compensation signal Δv_{cont} to the control signal v_{cont1} . The gate signal $GT2$ is obtained from the comparison of the control signal v_{cont2} and the triangular signals v_{tri2} . Due to the input inductor L and two diodes $D1$ and $D2$ in the three-level boosting PFC converter, both switches can be conducting at the same time without the concern of the short circuit damage. As plotted in Fig. 2, there are four switching states in the three-level boosting PFC converter. As shown in Fig. 2(a), both switches turn ON in the switching state 1. Thus, the inductor voltage v_L in the three-level

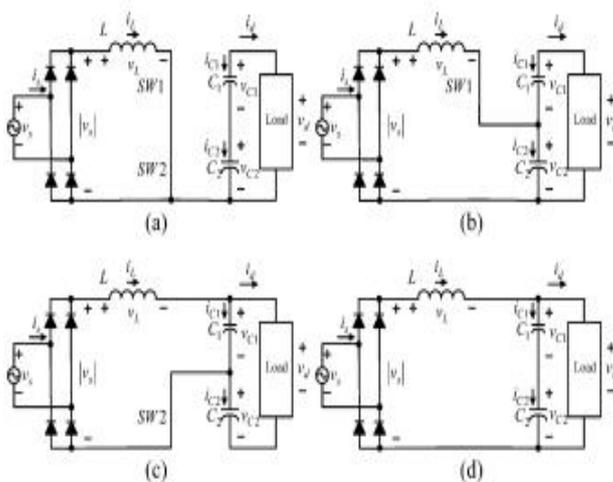


Fig. 2. Possible switching states in the three-level boosting PFC converter: (a) state 1, (b) state 2, (c) state 3, and (d) state 4

Table I capacitor currents in each state

		state 1	state 2	state 3	state 4
$2 > v_{cont1} + v_{cont2} > 1$	i_{C1}	$-i_d$ (<0)	$-i_d$ (<0)	$i_L - i_d$ (>0)	
	i_{C2}	$-i_d$ (<0)	$i_L - i_d$ (>0)	$-i_d$ (<0)	
$1 > v_{cont1} + v_{cont2} > 0$	i_{C1}		$-i_d$ (<0)	$i_L - i_d$ (>0)	$i_L - i_d$ (>0)
	i_{C2}		$i_L - i_d$ (>0)	$-i_d$ (<0)	$i_L - i_d$ (>0)

boosting PFC converter equals the rectified input voltage $v_L = |v_s|$ and both capacitors supply energy to the load $i_C 1 = i_C 2 = (-i_L) < 0$. In the switching state 2 in Fig. 2(b), the top switch turns ON and the bottom switch turns OFF. The resulting inductor voltage v_L equals the rectified input voltage $|v_s|$ minus the bottom capacitor voltage $v_L = |v_s| - v_{C2}$. Additionally, the capacitor C1 supplies energy to the load $i_C 1 = (-i_L) < 0$, but the capacitor C2 stores the energy from the input voltage $i_C 2 = (i_L - i_L) > 0$. Similarly, the resulting inductor voltage in Fig. 2(c) equals the rectified input voltage minus the top capacitor voltage $v_L = |v_s| - v_{C1}$. In the switching state 3, the top capacitor C1 is charged $i_C 1 = (i_L - i_L) > 0$, but the bottom capacitor C2 is discharged $i_C 2 = (-i_L) < 0$. When both switches turn OFF in Fig. 2(d), the resulting inductor voltage equals the rectified input voltage minus the output voltage $v_L = |v_s| - v_d = |v_s| - v_{C1} - v_{C2}$. The rectified input voltage $|v_s|$ supplies the load current and charges both capacitors simultaneously $i_C 1 = i_C 2 = (i_L - i_L) > 0$. All the capacitor currents in various switching states are tabulated in Table I. The behavior of the three-level boosting converter can be divided into two cases as shown in Fig. 3. In the case of $2 > v_{cont1} + v_{cont2} > 1$, two switches may conduct at the same time within the switching period T_s and there are switching state 1, state 2, and state 3. In the other case of $1 > v_{cont1} + v_{cont2} > 0$, only switching state 2, state 3, and state 4 exist.

III. PROPOSED METHOD AND RESULTS

The multi loop interleaved control and the proposed SCVBC with the proposed sampling/hold strategy are where only the input voltage v_s , the output voltage v_d , and the inductor current i_L are sensed. It is noted that the proposed sampling/hold strategy samples the inductor current i_L thrice per switching period T_s , and obtains the average value I_L and the other two values I_{vC1} and I_{vC2} . The average value current I_L is input to the multi loop control to yield the desired PFC function and obtain the control signal v_{cont1} . The difference ΔI_{vC} between two values I_{vC1} and I_{vC2} is calculated and the compensating signal Δv_{cont} is obtained by the used P controller. Then, the other control signal v_{cont2} is generated by adding the compensating signal Δv_{cont} to the control signal v_{cont1}

$$\Delta v_{cont} = K_p(I_{vC2} - I_{vC1}). \quad (6)$$

$$v_{cont2} = v_{cont1} + \Delta v_{cont} = v_{cont1} + K_p(I_{vC2} - I_{vC1}). \quad (7)$$

the proposed sampling/hold strategy with sensing the inductor current i_L . The average value I_L is obtained by sampling the inductor current i_L at the peak of the triangular signal $v_{tri1} = 1$. When the triangular signal v_{tri1} rises to 0.5 from the valley, the inductor current is sampled and the obtained.

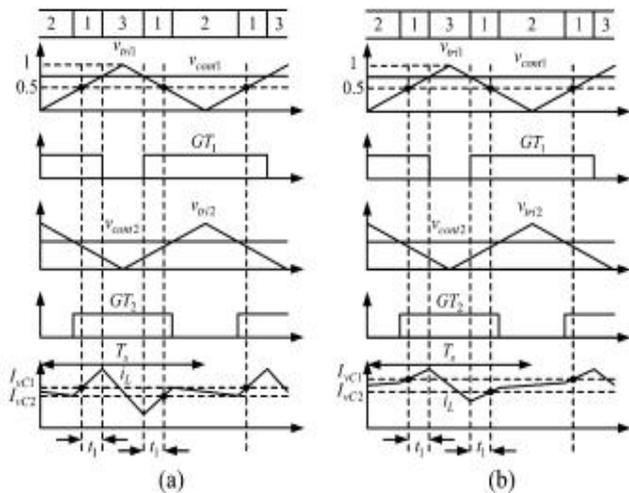


Fig. 7. Illustrated waveforms ($2 > v_{cont1} + v_{cont2} > 1$). (a)

$v_{C1} > v_{C2} > |v_s|$ and (b) $v_{C1} > |v_s| > v_{C2}$ Value is defined as I_{vC1} . The value I_{vC2} is sampled when the triangular signal v_{tri1} falls to 0.5 from the peak. After finishing all the sampling actions, the multi loop control is performed at the controller time, and updates the two control signals at the valley of the triangular signal v_{tri1} . In the following paragraphs, the analysis is divided into two cases - $2 > v_{cont1} + v_{cont2} > 1$ and $1 > v_{cont1} + v_{cont2} > 0$. The illustrated waveforms for the voltage imbalance $\Delta v_C > 0$ (i.e., $v_{C1} > v_{C2}$) are plotted in. Since the input ac voltage v_s is time-varying, the voltage imbalance $\Delta v_C > 0$ may be divided into two conditions—either $v_{C1} > v_{C2} > |v_s|$ or $v_{C1} > |v_s| > v_{C2}$. The waveforms in the condition $v_{C1} > v_{C2} > |v_s|$ are plotted in, and the inductor current i_L is falling at the switching state 2. But the inductor current i_L is rising at the switching state 2 in the other condition $v_{C1} > |v_s| > v_{C2}$ as plotted in. The illustrated waveforms for

the voltage imbalance $v_{C2} > v_{C1} > |v_s|$ and $v_{C2} > |v_s| > v_{C1}$ are plotted in respectively. It is noted that in, the inductor current i_L is falling at the switching state 3, but the current i_L is rising at the switching state 3 in. Due to the waveform symmetry in, the time t_1 between the instants of sampling the value I_{vC1} and the turning-off instants of the gate signal GT_1 is equal to the time between the turning-on instants of the gate signal GT_1 and the instants of sampling the value I_{vC2} . Therefore, the time t_1 can be expressed in terms of the control signal v_{cont1}

$$t_1 = \left(\frac{v_{cont1}}{2} - \frac{1}{4} \right) T_s. \quad (8)$$

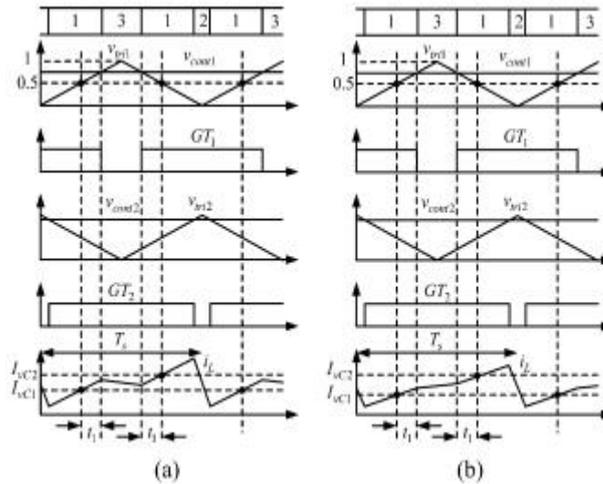


Fig. 8. Illustrated waveforms($v_{C2} > v_{cont1} + v_{cont2} > 1$). (a)

$v_{C2} > v_{C1} > |v_s|$ and (b) $v_{C2} > |v_s| > v_{C1}$. the conducting time for the switching state 2 and the switching state 3 are $(1 - v_{cont2})T_s$ and $(1 - v_{cont1})T_s$, respectively. The remaining time for switching state 1 is $(v_{cont1} + v_{cont2} - 1)T_s$. Then, the average inductor voltage $v_L T_s$ in the three-level boosting converter can be expressed as equation (9) at the bottom of the page. Because of zero average inductor voltage in the steady-state condition, the rectified input voltage $|v_s|$ must be equal to

$$|v_s| = (1 - v_{cont1})v_{C1} + (1 - v_{cont2})v_{C2}. \quad (10)$$

the difference ΔI_{vC} between two sampled values I_{vC1} and I_{vC2} can be expressed in terms of the time t_1

$$\Delta I_{vC} = I_{vC2} - I_{vC1} = 2 \frac{|v_s|}{L} t_1 + \frac{|v_s| - v_{C1}}{L} (1 - v_{cont1}) T_s. \quad (11)$$

Substituting (8) and (10) into (11) obtains

$$\Delta I_{vC} = \frac{T_s}{2L} [(v_{C2} - v_{C1})(1 - v_{cont1}) - \Delta v_{cont} v_{C2}]. \quad (12)$$

By substituting (6) into (12), the expression ΔI_{vC} in (12) can be rewritten as Because the coefficient k_1 is always positive, the difference ΔI_{vC} is proportional to the voltage imbalance $(v_{C2} - v_{C1})$. It follows that the difference ΔI_{vC} can be used to detect the voltage imbalance $(v_{C2} - v_{C1})$ without directly sensing the capacitor voltages. $1 > v_{cont1} + v_{cont2} > 0$

$$\Delta I_{vC} = \frac{I_s(1 - v_{cont1})}{2L + T_s K_P v_{C2}} (v_{C2} - v_{C1}) = k_1 (v_{C2} - v_{C1}). \quad (13)$$

$$\langle v_L \rangle_{T_s} = \frac{|v_s|(v_{cont1} + v_{cont2} - 1)T_s + (|v_s| - v_{C1})(1 - v_{cont1})T_s + (|v_s| - v_{C2})(1 - v_{cont2})T_s}{T_s}$$

$$= |v_s| - v_{C1}(1 - v_{cont1}) - v_{C2}(1 - v_{cont2}) \quad (9)$$

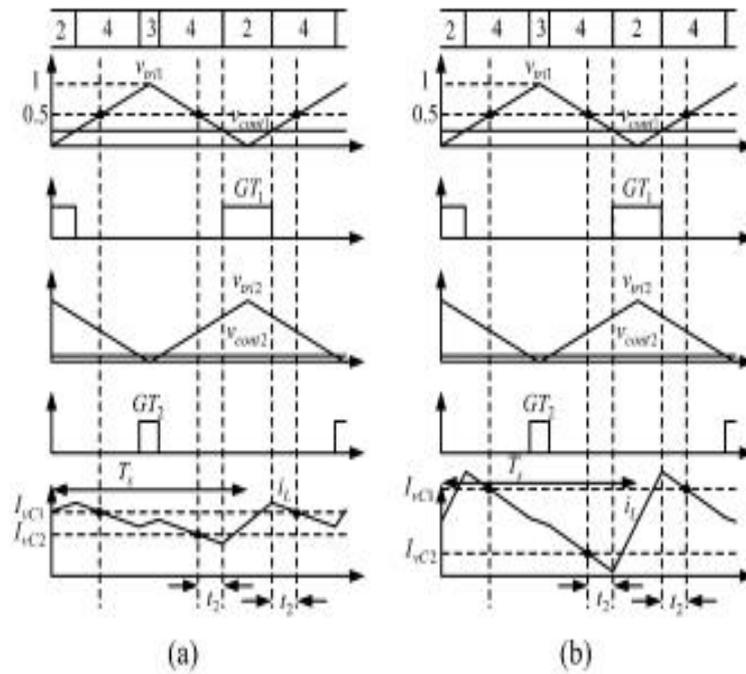
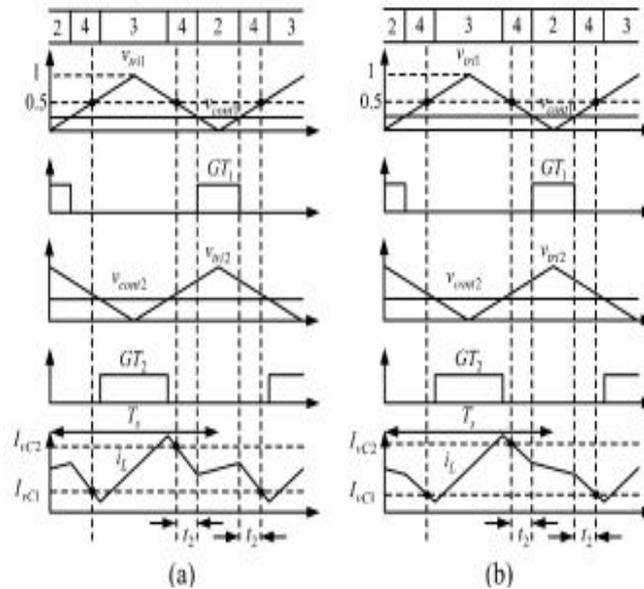


Fig. 9. Illustrated waveforms ($1 > v_{cont1} + v_{cont2} > 0$). (a) $|v_s| > v_{C1} > v_{C2}$ and (b) $v_{C1} > |v_s| > v_{C2}$.



Illustrated waveforms ($1 > v_{cont1} + v_{cont2} > 0$). (a) $|v_s| > v_{C2} > v_{C1}$ and (b) $v_{C2} > |v_s| > v_{C1}$. In this case, the illustrated waveforms for the voltage imbalance $v_{C1} > v_{C2} > |v_s|$ and $v_{C1} > v_{C2} > |v_s|$ are plotted respectively. In the inductor current i_L is rising at the switching state 3, but the inductor current i_L is falling at the switching state 3. The illustrated waveforms for the voltage imbalance $|v_s| > v_{C2} > v_{C1}$ and $v_{C2} > |v_s| > v_{C1}$ are plotted respectively. It is noted that in the inductor current i_L is rising at the switching state 2 due to $|v_s| > v_{C2}$, but the current i_L is falling at the switching state 2 in due to $v_{C2} > |v_s|$.

$$t_2 = \left(\frac{1}{4} - \frac{v_{cont1}}{2} \right) T_s. \quad (14)$$

The coefficient k_2 may be either positive one or negative one. In order to force the coefficient k_2 positive, the denominator should be positive. It implies that the controller parameter K_P should be located at the range

$$2L - T_s K_P v_{C2} > 0. \tag{19}$$

$$0 < K_P < \frac{2L}{T_s v_{C2, \max}} \tag{20}$$

Where $v_{C2, \max}$ is the maximum bottom capacitor voltage. Then, the difference Δv_C would be proportional to the voltage imbalance ($v_{C2} - v_{C1}$). From (13) and (18) in both cases, the difference Δv_C in both cases are proportional to the voltage imbalance ($v_{C2} - v_{C1}$) via properly selecting the controller parameter K_P , which implies that the difference Δv_C obtained from the proposed SCVBC can be used to detect the voltage imbalance ($v_{C2} - v_{C1}$) without directly sensing the capacitor voltages.

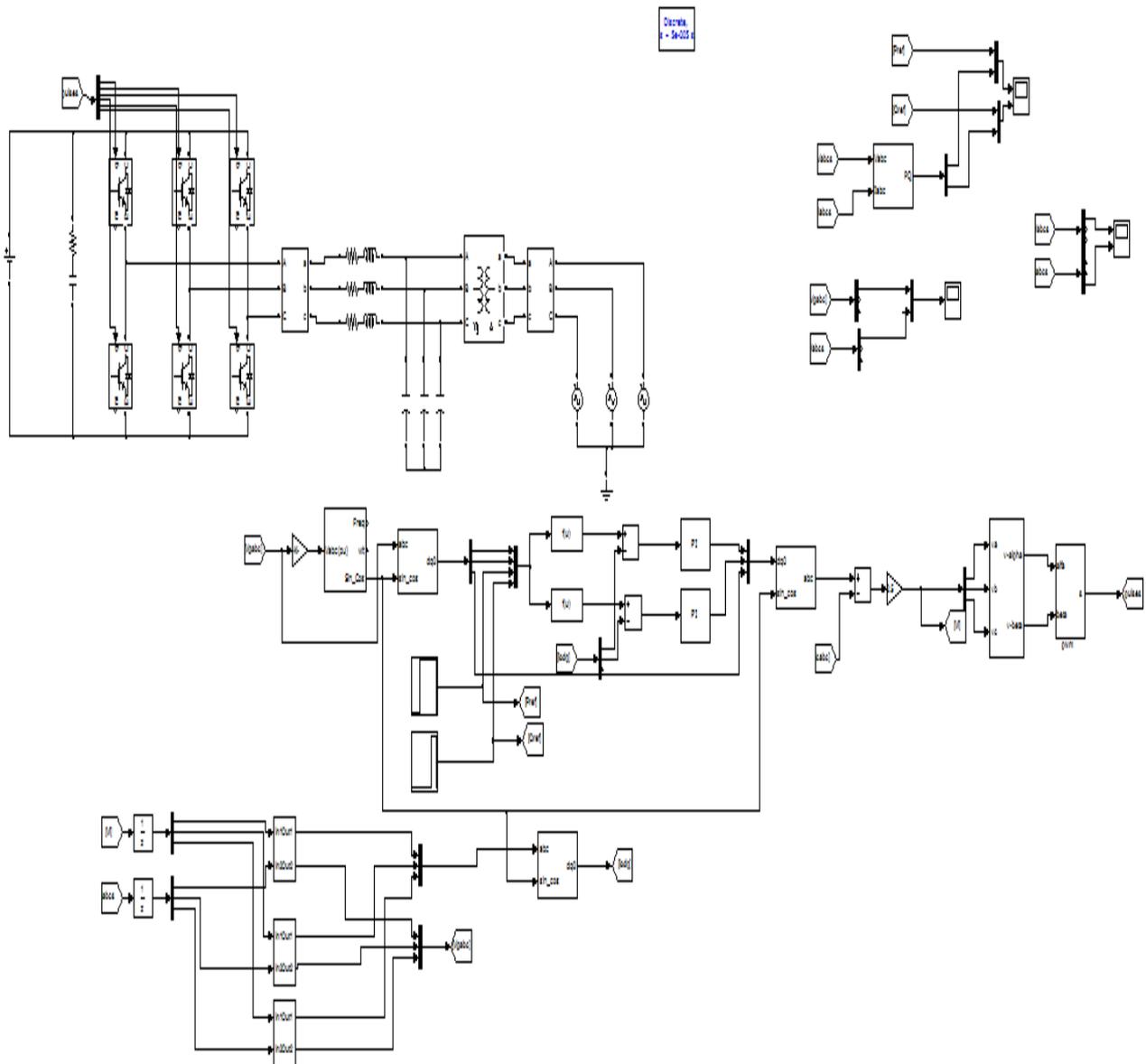
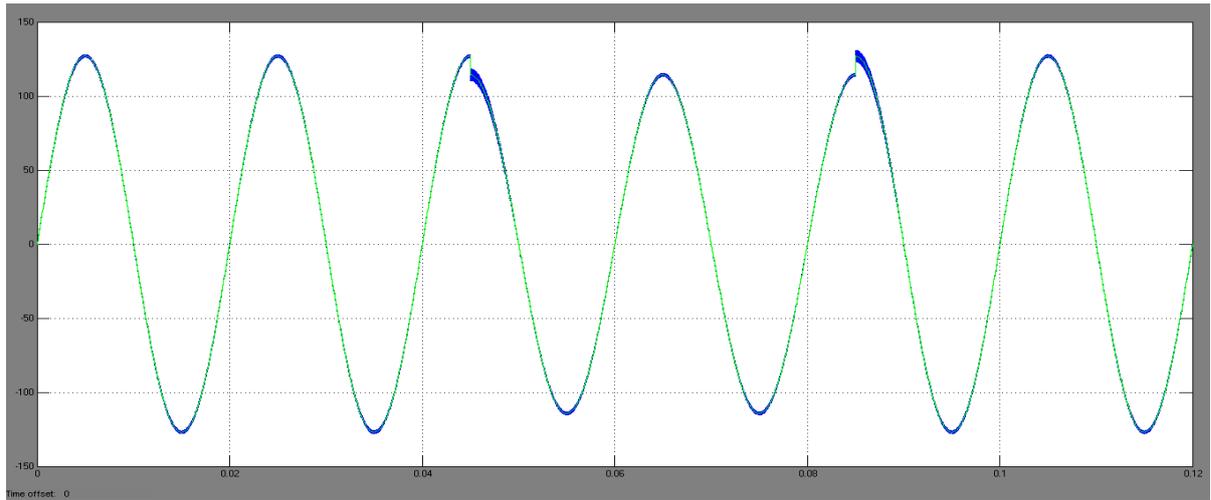
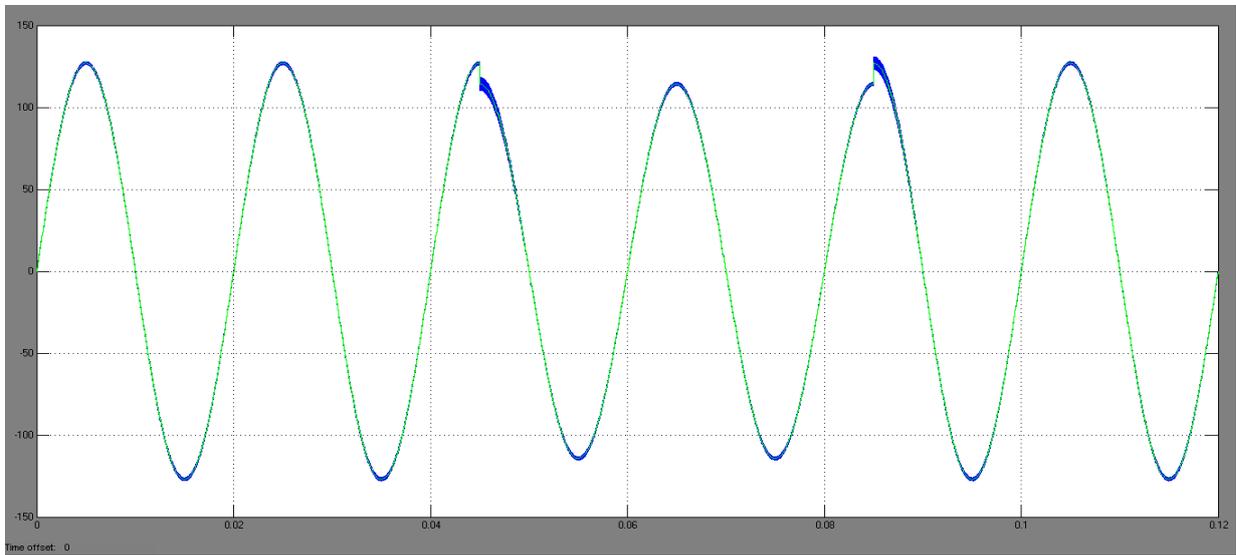


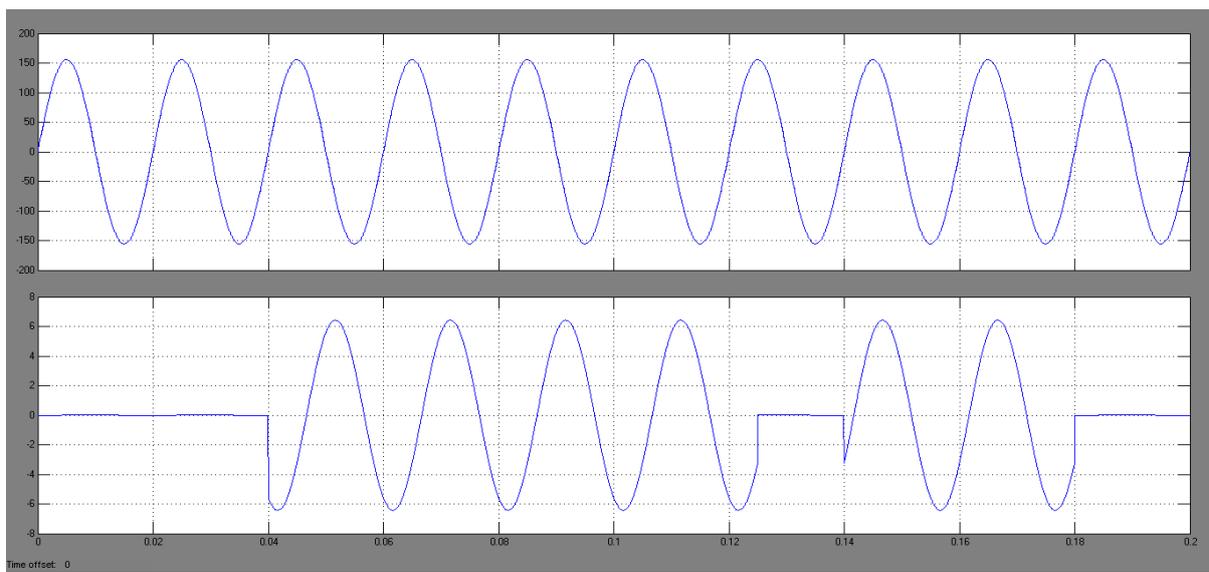
Fig. 16. Block diagram of the implemented three-level boosting PFC converter



(a)



(b)



(c) - system dynamics under different power conditions

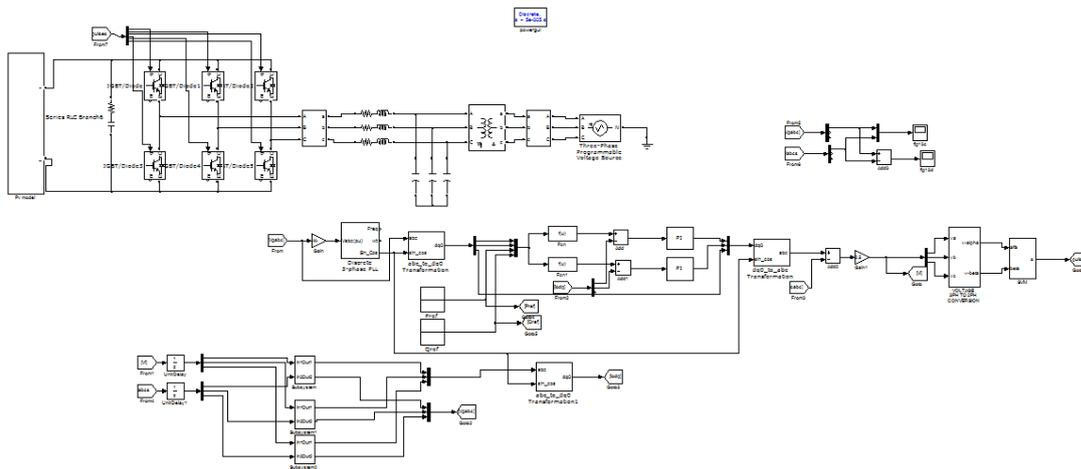


Fig. 17 Block diagram of the implemented three-level boosting PFC converter with PV system

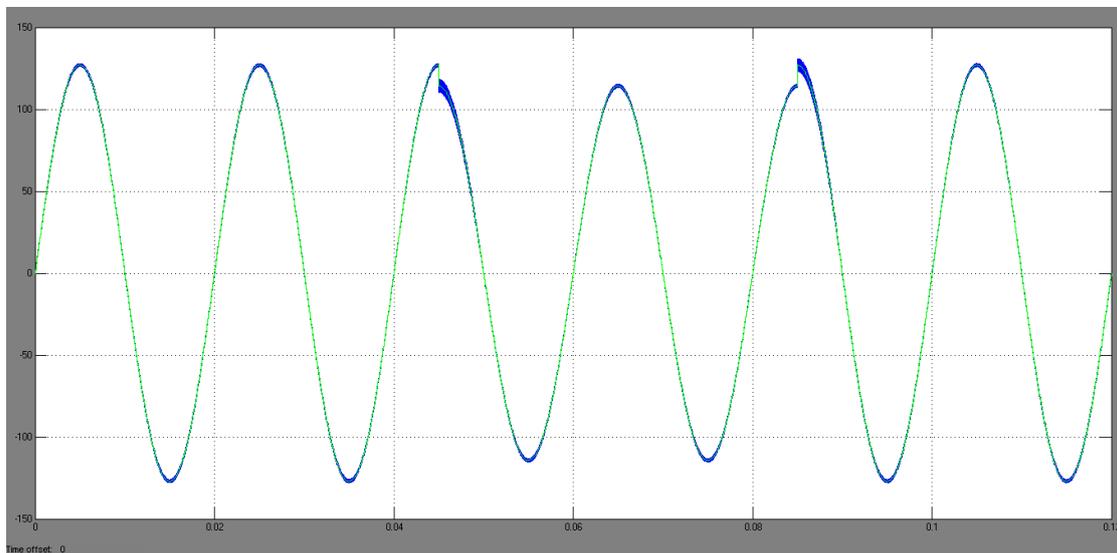


Fig. 18 system dynamics under different power conditions with PV system

CONCLUSION

In this paper, the SCVBC method for the three-level boosting PFC converter has been proposed. The proposed method shows that the voltage imbalance can be detected from sensing the inductor current by the proposed sampling/hold strategy. That is, it eliminates the need for extra sensors, reduces control complexity, and reduces the cost and size. The reduction of cost and size are the important contributions for PFC converters. The control method is implemented in an FPGA-based system, and all the provided results demonstrate the proposed method. The PV system operated under different conditions also performed.

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