Analysis of converter topologies with respect to Harmonic distortion used for grid connected single phase transformer less PV system

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***Abstract*—In this paper analysis of 2-level inverter, 3-level NPC (Neutral Point Clamped) inverter, 3-level cascaded inverter, 5-level inverter, 7-level inverter and 9-level inverter topologies in different aspects. Basic comparison is on THD, output voltage and no. of devices connected to the circuit and accordingly changes.**

IndexTerms—Neutral point clamped (NPC) inverter, Total harmonic distortion (THD), Photovoltaic (PV) system

I. INTRODUCTION

In general, the multilevel converters are applied to the medium voltage application such as the power converter for large power motor drive and also for power transmission line. Because, the multilevel converter can reduce the voltage stress of a switching device to 1/(n-1) of the DC input voltage and also reduce the harmonic component of the output voltage. Recently, low voltage applications also has been studied to apply the multilevel converters for high efficiency such as in the uninterrupted power supply (UPS) and power converter for photo voltaic cell (PV) . There are two conventional multilevel topologies; the neutral point clamped (NPC) type and the flying capacitor (FC) type. NPC topology outputs the voltage level from the neutral point voltage that is clamped by using the diodes. However the number of switching devices increases in proportional to the voltage level. FC topology outputs the voltage level from the DC link voltage by adding the flying capacitor voltage. However, FC topology requires more capacitors as the voltage level increased. Loss analysis by using simulator is a simple method to study the losses among the multilevel converter topologies under a same device specification. However the loss estimation by simulation is not useful to optimize the optimization of design because hundreds of simulations are required under different conditions. The performance comparison among the four converters shows that the 9-level cascaded inverter can achieve the highest efficiency and 3-level NPC inverter is only useful because after 3-level for 5-level NPC topology is become too complex so NPC topology give best result on 3-level. So after 3-level NPC inverter 5-level, 7-level, 9-level and so on preferred cascaded inverter topology.

In light of public concern about global warming and climate change, much effort has been focused on the development of environmentally friendly distributed energy resources (DERs). For delivering premium electric power in terms of high efficiency, reliability, and power quality, integrating interface converters of DERs such as photovoltaic (PV), wind power, microturbines, and fuel cells into the microgrid system has become a critical issue in recent years. In such systems, most DERs usually supply a dc voltage that varies in a wide range according to various load conditions. Thus, a dc/ac power processing interface is required and is compliable with residential, industrial, and utility grid standards various converter topologies have been developed for DERs that demonstrate effective power flow control performance whether in grid-connected or stand-alone operation. Among them, solutions that employ high-frequency transformers omitted no use of transformers at all have been investigated to reduce size, weight, and expense. For low-medium power applications, international standards allow the use of grid-connected power converters without galvanic isolation, thus allowing so called “transformerless” architectures Furthermore,as the output voltage level increases, the output harmoniccontent of such inverters decreases, allowing the use of smallerand less expensive output filters. As a result, various multileveltopologies are usually characterized by a strong reduction inswitching voltages across power switches, allowing the reductionof switching power losses and electromagnetic interference(EMI).

A single-phase multistring five-level inverter integrated with an auxiliary circuit was recently proposed for dc/ac power conversion. This topology used in the power stage offers an important improvement in terms of lower component count and reduced output harmonics. Unfortunately, high switching losses in the additional auxiliary circuit caused the efficiency of the multistring five-level inverter to be approximately 4% less than that of the conventional multistring three-level inverter.

II. DIFFERENT CONVERTER TOPOLOGIES:

Fig. 1 shows the block diagram of transformer less PV system. In proposed topology we are using PV system as a input so we need inverter for converting output of PV array which is DC into AC and then given to the grid. Now for analyzing different converter topologies we have to compare it on various aspects.

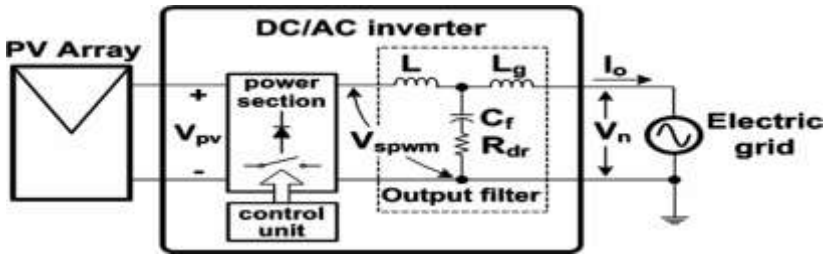

Fig.1.Block diagram of a transformer less PV inverter

Fig. 1shows the block diagram of a transformer less PV inverter system. This converter architecture was originally developed, in combination with a suitable PWM modulation strategy, inorder to keep constant the output common mode voltage incase of a full bridge converter architecture driven by aUnipolar modulation.In this paper this converter structure is used to develop a fivelevel grid connected converter for single phase applications.In steady state conditions, due to the low voltage dropacross the inductances Lf of the output filter, the outputvoltage of the converter has a fundamental component veryclose to the grid voltage. The frequencies of these twovoltages are identical while the amplitudes and their phasedisplacement are only slightly different. As a consequence,the shape of the modulation index, m, of the power converteris very similar to the grid voltage waveform as well. Underthis assumption the output voltage of the converter can bewritten as Vout= m·VDC.

Three single-phase, two-level voltage source converters can be connected to the same capacitor to form a three phase converter. This converter power circuit arrangementis often called the six-pulse converter configuration (Figure 2). In this circuit, the switches in one leg are switched alternatively with a small dead time to avoid both conducting simultaneously. Therefore, one switching function is enough to control both switches in a leg.

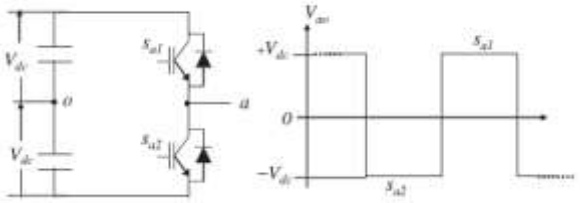

Fig. 2. Fundamental principles of a single-phase, two-level converter

There are a number of different switching strategies for VSIs. These include square-wave operation, carrier-based pulse-width modulation (CB-PWM) techniques such as switching frequency optimal PWM (SFO-PWM), sinusoidal regular sampled PWM (RS-PWM), non- regular sampled PWM (NRS-PWM), selective harmonic elimination PWM (SHEM), space vector PWM (SV-PWM) and hysteresis switching techniques.

TABLE I
COMPARISON OF AN M-LEVEL INVERTER ACCORDING TO TOPOLOGIES

	Single Phase Topologies		Three Phase Topologies		
	Half Bridge	Full Bridge	Diode Clamped	Flying Capacitor	Cascaded
THD_V (%)	163	156	36,9	33,1	32,4
Main power switches per phase	2	4	2(m-1)	2(m-1)	2(m-1)
Clamping diodes per phase	0	0	(m-1).(m-2)	0	0
DC bus capacitor	2	2	(m-1)	(m-1)	(m-1)/2
Balancing capacitor per phase	0	0	0	(m-1).(m-2)/2	0
Total material for m=5	-	-	24	18	10
Control Scheme	Regular PWM	Regular PWM	SHE-PWM, SPWM, SVM	SHE-PWM, SPWM	SPWM, SVM
Applications	< 2kV	< 2kV	Motor drive, STATCOM	Motor drive., STATCOM	PV, Motor drive, STATCOM, Batteries

III. OPERATION STRATEGY:

The objective of this paper is to develop a robustly designed inverter block with mathematical model for SPWM modulator to minimize THD ratios and compare to other conventional models. The inverter output values will be discussed for several switching frequencies and modulation indexes applied to modulator. The results obtained from simulation of Matlab- Simulink shows that the harmonic contents are greatly reduced by using mathematically well designed SPWM modulator.

II. GENERAL CASCADED TOPOLOGY or MULTILEVEL INVERTER

A. Basic Principle of Multilevel Inverter" and Application to Design

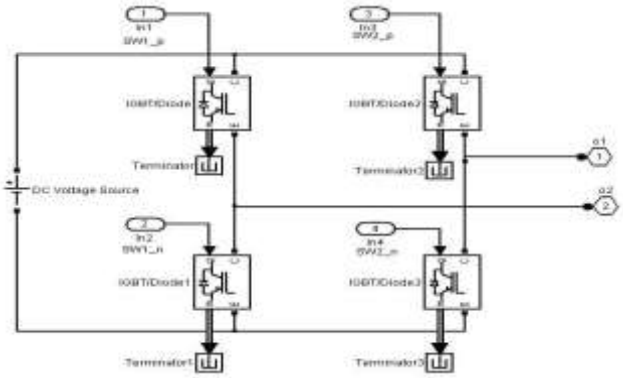

Fig. 3.main H-bridge cell of inverter

Fig. 3 shows the main H-bridge cell of one inverter used for implementation of the multilevel inverter. The full bridge inverter module includes four power switches and four clamping diodes to form an H-bridge. A multilevel cascade inverter consists a number of H»bridge cells that connected series per phase, and each module requires a separate DC source to generate voltage levels at the output of inverter. The switching inputs shown as lmvi in the Fig. 3 will allow obtaining output voltages of each H-bridge as follows:

$$V_{out} = \begin{cases} +V_{dc} & In1, In4 \quad on \\ 0V_{dc} & In1, In3 \quad on \\ -V_{dc} & In2, In3 \quad on \end{cases} \qquad (1)$$

IV. HARMONIC ANALYSIS AND SIMULATION:

The mathematical model of SPWM modulator has been developed in Simulink and the success on harmonic preventing has been compared to the conventional model. The SPWM modulator has a switching bandwidth between 0- 40 KHZ to control H-bridges and Fig. 7 shows the values which are obtained at 5 KHZ switching conditions while m,= 1.
Following graphs represent the FFT analysis of the current THD (THDi) and voltage THD (THDV) ratios in Simulink. The switching frequency of SPWM modulator has been limited to 1-10 KHZ, and modulation indexes are selected in 0.65 mi 1.4 range to analyze the effect of fw and m, on THD of inverter. It has been observed by the performed tests that reducing the THD of current and voltage is depended on increasing the

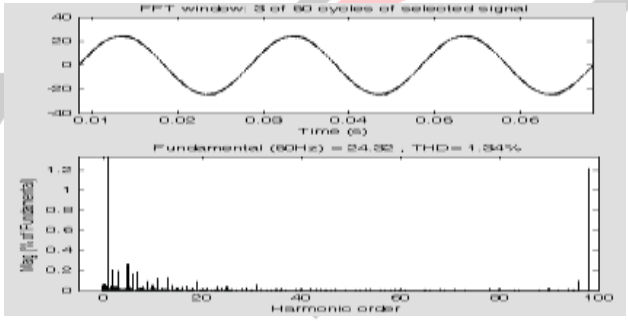

Fig.4. a) and b) FFT window and harmonic order:

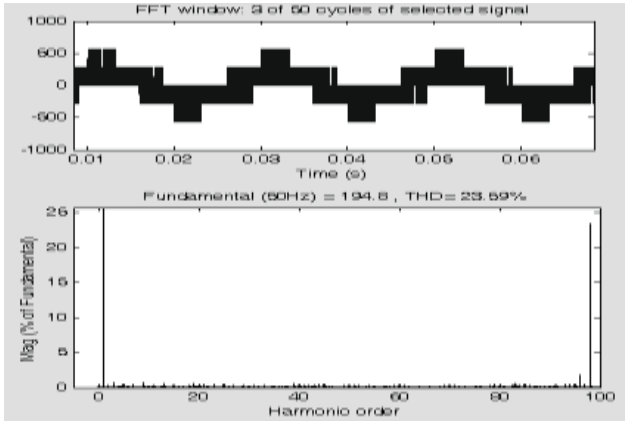

Fig. 5.a) and b) FFT window and harmonic order:

switching frequency in linear modulation range as shown in Fig. 5 (a) and Fig. 5 (b) respectively. The output current and voltage values have been increased in over-modulation range since m, is over 1, but the THD rates have been changed nonlinearly. The lowest THD for current has been measured as 0.1% during 10 KHZ switching frequency and m,= 0.8 conditions. The THD for voltage has been measured as 0.66% under same conditions as shown in Fig. 5 (b). Fig. 4 (a) represents a pattern of FFT analyses, which have been performed to constitute the Fig. 4 (a) and (b), for current THD at 10 KHZ switching frequency. Fig. 5 (b), as another example, shows the THD for current at l KHZ switching frequency, and the modulation index is l for both. The lower switching frequency in linear modulation range has caused to higher THD for current and voltage at the inverter output.

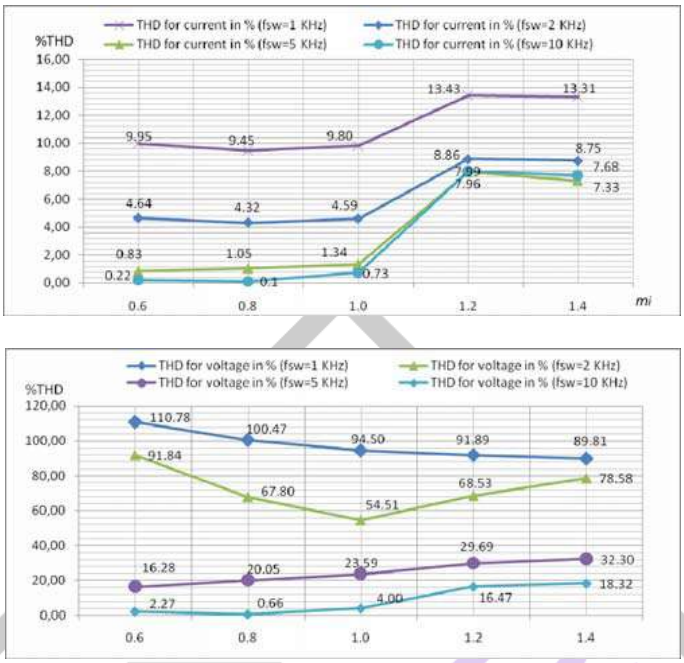

Fig.6. THD analysis of inverter at various switching frequencies and modulation indexes (a) THD for current in % (b) THD for phase voltages in %

V.

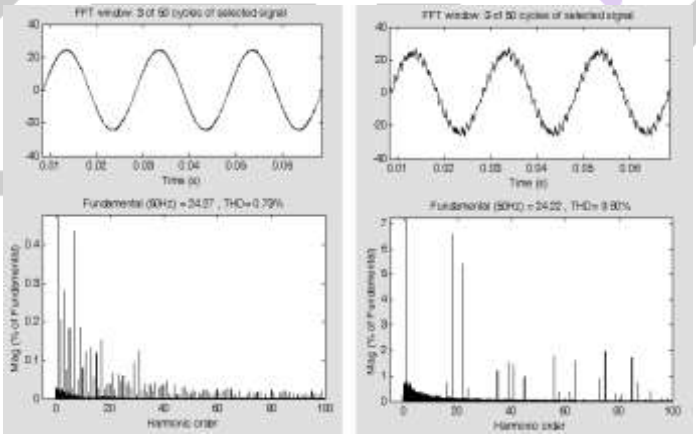

Fig.7. THD current analysis while m=l (a) THD for current is 0.73% at 10 KHZ switching (b) THD for current is 9.80 % at 1 KHZ switching 579

VI. CONCLUSION

This paper cascaded H-bridge Seven level inverter using low frequency transformers with single DC source is proposed. The proposed circuit produces required seven level output voltage having low harmonics with reduced number of components when compared to conventional methods. Harmonic spectrum for seven level output voltage is analyzed to prove its efficiency in reducing output harmonic components. Simulated and experimental output Waveforms were shown to prove the reliability and feasibility of the circuit.

The measurement results have presented perfect outcomes on THD analysis. The modulation indexes in over modulation range have caused non linear changes in THD values of output current and voltages but on the other hand, the TI-ID of output current and voltages have seen extremely low in linear modulation range according to IEEE 519-1992 (THD<5%). It is also seen that the switching frequency is directly effective on THD. The increment in switching frequency has showed its reducer effect on THD of

output current and voltages. In addition, the measured harmonic contents have seen as fundamental (50 HZ, 1*‘), 96"“and 98"“harmonics in 5 KHz and 10 KHz switching conditions of linear modulation area (m,S1). The harmonic contents of current, which have measured by using modulation at 2 KHZ and over, have seen as lower order harmonics and magnitudes have measured lower than 0.2 A.

The THD of output voltage has been measured lower than 24% in linear modulation band, and the most effective harmonic contents except fundamental wave have seen at 96"‘ and 98"“ as in analysis of output current. The accuracy of design will be verified with the results of continuing experimental studies.

It has been advantages of like reduction in phase current, reliable in faulty conditions, reduction in current ripple as comparison between TPTLVSI and FPTLVSI, It can encourage of reduction of current rating of switches like IGBTS/MOSFET used in Voltage source inverters.

A comparison of total harmonic distortion in the output phase voltages of five-phase voltage source inverter for different conduction angle is presented. The conduction angles considered are 180°, 162°, 144°, 126°, and 108°. Thus two more conduction states are included when compared to further prove the superiority of control at 120° conduction mode. It is observed that the lowest THD is obtained for 120° conduction mode.

This paper has reviewed analytical approach for five phase two level voltage inverter used in application of induction motor drive.

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