A Modified Topology of 3-phase 4-wire UPQC for Power Quality Improvement

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***Abstract*: A UPQC (Unified Power Quality Conditioner) is a custom power device, which reduces voltage and current-related PQ issues in the power distribution systems. This paper proposes UPQC topology for applications with non-stiff source. This topology enables UPQC to have a reduced dc-link voltage without compromising its compensation capability. This helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. In this method, a capacitor is connected in series with the interfacing inductor of the shunt active filter. The system neutral is connected to the negative terminal of the dc-link voltage. This connection avoids the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter. Therefore, the average switching frequency of the switches in the VSI also reduces. Due to this the switching losses in the inverters reduce. A simulation study of the proposed topology has been carried out using MATLAB 2016a and the results are presented. Experimental design is developed three-phase UPQC prototype to verify the proposed topology.**

1. Introduction

Nowadays, Renewable sources are increasingly used for electricity generation. Due to power electronics & digital control technology, the renewable energy sources are connected to the distribution systems. But power electronics devices, nonlinear loads & unbalanced loads decrease power quality (PQ) in distribution network. To enhance power quality custom power devices like UPQC are used. The UPQC (Unified Power Quality Conditioner) consists of two inverters connected back-to-back which deals with both load current & supply voltage imperfections.

UPQC can simultaneously act as shunt & series active power filters. The series part is a dynamic voltage restorer (DVR). It is used to maintain balanced, distortion free nominal voltage at the load. The shunt part of UPQC is called as distribution static compensator (DSTATCOM). It is used to compensate reactive power & harmonics. It also balances the load currents; therefore, it makes the source current balanced & distortion free with unity power factor.

Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter. The dc-link voltage for the shunt active filter should be greater than the peak value of the line-to-neutral voltage. It is needed to ensure a proper compensation at the peak of the source voltage. The dc-link voltage should be greater than or equal to √6 times the phase voltage of the system for distortion free compensation. For reactive power compensation, the magnitude of reference dc-bus capacitor voltage should be higher than the peak voltage at the point of common coupling (PCC). Therefore, the higher value of dc capacitor voltage is used. For series, active filter, the dc-link voltage should be equal to the peak of the line-to-line voltage of the system for proper compensation.

The dc-link voltage requirement for the shunt and series active filters is different for UPQC. Therefore, it is very necessary maintain a common dc-link of appropriate rating which will satisfy shunt and series compensation. The shunt active filter requires greater value of dc-link voltage. As compared to this, series active filter requires less value of dc link voltage for proper compensation. If common dc link voltage based on shunt active filter requirement is selected, it will cause over rating of the series active filter. If the higher dc link voltage is selected, it requires high value of dc link capacitor. Due to this the voltage

source inverters (VSIs) become bulky and its switches need to be rated for higher value of voltage and current. Ultimately it increases entire cost and size of VSI. To reduce the dc-link voltage storage capacity, a hybrid filter has been discussed for motor drive applications in [2], [3]. The filter is connected in parallel with diode rectifier and tuned at seventh harmonic frequency. But this design is only for the motor drive application, and it does not consider the reactive power compensation.

A neutral-clamped topology is used for three-phase four-wire system for UPQC in [4], [5]. This topology enables the independent control of each leg of both the shunt and series inverters, but it requires capacitor voltage balancing. A four-leg VSI topology for shunt active filter has been discussed in [7] for three-phase four-wire system. This topology does not control voltage balancing of the capacitor, but the independent control of the inverter legs is not possible. To overcome the problems associated with the four-leg topology, in [8], [9], the authors proposed a T-connected transformer and three-phase VSC based DSTATCOM. However, this topology increases the cost and bulkiness of the UPQC because of the presence of extra transformer.

This paper explains UPQC topology with reduced dc-link voltage. It consists of capacitor in series with the interfacing inductor of the shunt active filter. The benefit of series capacitor it reduces in dc-link voltage requirement of the shunt active filter and simultaneously compensates the reactive power required by the load. Due to this unity power factor is maintained without compromising its performance. This matches the dc-link voltage requirements of the series and shunt active filters with a common

dc-link capacitor. In this topology, the system neutral is connected to the negative terminal of the dc bus. This will avoid the requirement of the fourth leg in VSI of the shunt active filter and enables independent control of each leg of the shunt VSI with single dc capacitor. The simulation studies are carried out using MATLAB 2016a and detailed results are presented in the paper. A prototype of three-phase UPQC is developed in the laboratory to verify the proposed concept, and the detailed results are presented in this paper.

2. CONVENTIONAL AND MODIFIED TOPOLOGIES OF UPQC

The conventional and proposed topologies of the UPQC are discussed in detail. Fig. 1

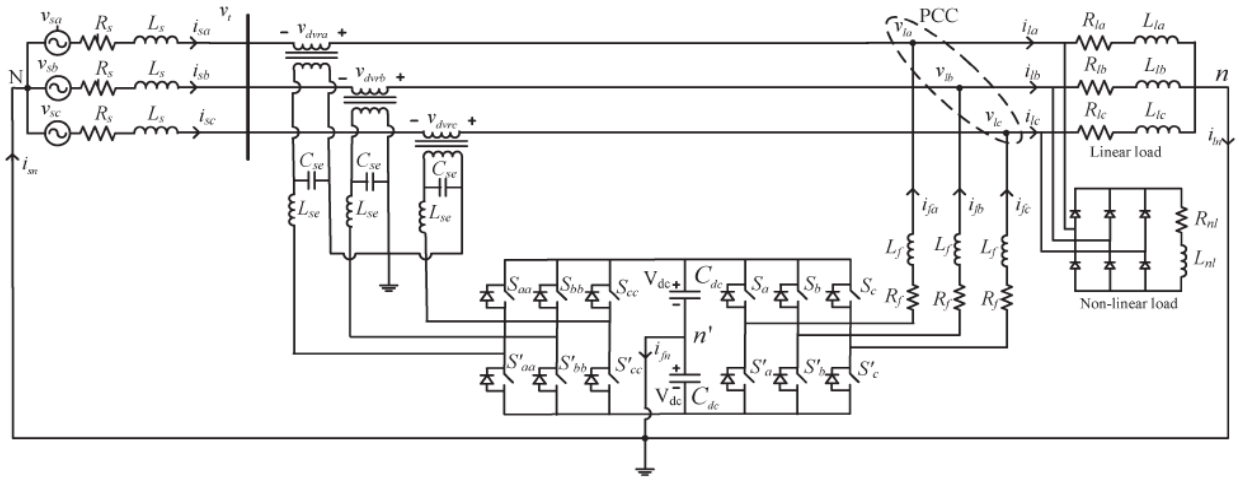

Fig. 1 Equivalent circuit of neutral-clamped VSI topology-based UPQC.

Fig. 1 shows the power circuit of the neutral-clamped VSI topology-based UPQC which is considered as the conventional topology. This topology requires two dc storage devices, each leg of the VSI can be controlled independently, and tracking is smooth with less number of switches when compared to other VSI topologies [6]. In this figure, *vsa*, *vsb*, and *vsc* are source voltages of phases *a*, *b* and *c*, respectively. Similarly, *vta*, *vtb*, and *vtc* are terminal voltages. The voltages *v*dvr*a*, *v*dvr*b*, and *v*dvr*c* are injected by the series active filter. The three phase source currents are represented by *isa*, *isb*, and *isc*, load currents are represented by *ila*, *ilb*, and *ilc*. The shunt active filter currents are denoted by *ifa*, *ifb*, *ifc*, and *iln* represents the current in the neutral leg. *Ls* and *Rs* represent the feeder inductance and resistance, respectively. The interfacing inductance and resistance of the shunt active filter are represented by *Lf* and *Rf* , respectively, and the interfacing inductance and filter capacitor of the series active filter are represented by *L*se and *C*se, respectively. The load constituted of both linear and nonlinear loads as shown in this figure. The dc-link capacitors and voltages across them are represented by *C*dc1 = *C*dc2 = *C*dc and *V*dc1 = *V*dc2 = *V*dc, respectively, and the total dc-link voltage is represented by *Vd*bus (*V*dc1 + *V*dc2 = 2*V*dc). In this conventional topology, the voltage across each common dc-link capacitor is chosen as 1.6 times the peak value of the source voltages as given in [6].

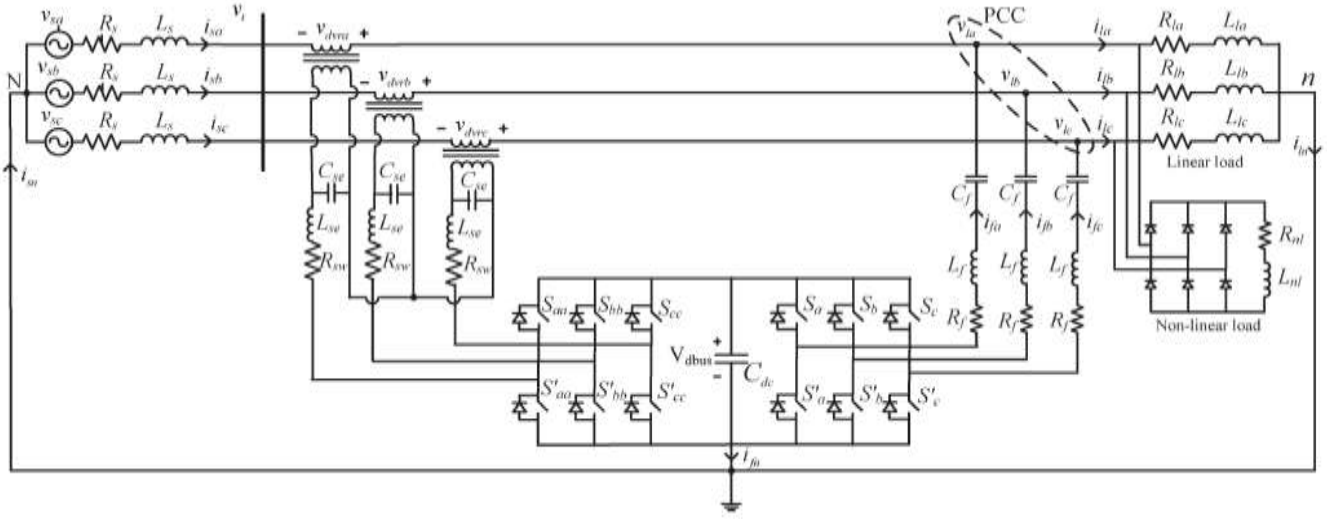

Fig. 2. Equivalent circuit of proposed VSI topology for UPQC compensated system (modified topology)

Fig. 2 represents the equivalent circuit of the proposed VSI topology for UPQC compensated system. In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor *Cf* in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitor *Cf* will supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. The reduction in the dc-link voltage requirement of the shunt active filter enables to the match the dc-link voltage requirement with the series active filter. This topology avoids the over rating of the series active filter of the UPQC compensation system. The design of the series capacitor *Cf* and the other VSI parameters have significant effect on the performance of the compensator. This topology uses a single dc capacitor which avoids the need of balancing the dc-link voltages. Each leg of the inverter can be

controlled independently in shunt active filter. This topology does not require the fourth leg in the shunt active filter for three-phase four-wire system. The performance of this topology is explained in detailed in the following section.

3. VSI COMPONENTS DESIGN

The specifications of components of the VSI are designed carefully for better tracking performance. The important parameters of conventional VSI are *V*dc, *C*dc, *Lf* , *L*se, *C*se, and switching frequency (*f*sw). The design details of the VSI parameters for the shunt and series active filter are given in [10], [11].

3.1 Design of Shunt Active Filter VSI Parameters

Consider the active filter is connected to an X kVA system and deals with 0.5X kVA and 2X kVA handling capability under transient conditions for *n* cycles. During transient, with an increase in system kVA load, the voltage across each dc-link capacitor (*V*dc) decreases and vice versa. Allowing a maximum of 25% variation in *V*dc during transient, the differential energy (Δ*Ec*) across *C*dc is given by

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$$\Delta E_c = \frac{C_{dc}\left[(1.125V_{dc})^2 - (0.875V_{dc})^2\right]}{2} \quad \textbf{-(1)}$$

The change in system energy (Δ*Es*) for a load change from 2X kVA to 0.5X kVA is given by

$$\Delta E_s = (2X - X/2)nT. \quad \textbf{----------(2)}$$

Equating (1) and (2), the dc-link capacitor value is given by

$$C_{dc} = \frac{2(2X - X/2)nT}{(1.125V_{dc})^2 - (0.875V_{dc})^2} \textbf{---(3)}$$

where, *Vm* is the peak value of the source voltage, *X* is the kVA rating of the system, *n* is number of cycles, and *T* time period of each cycle.

An empirical study has been carried out for various values of interfacing inductance values with the variation of the dc-link voltage in [31], with *V*dc = *mVm*, and it is found that *m* = 1.6 gives fairly good switching performance of the
VSI. The approximate relationship between *m* and minimum (*f*swmin), maximum switching frequency (*f*swmax) is obtained by analysis of the VSI in [10], and this is given below. For switching frequency variation approximately from 6 kHz to 10 kHz, the value of m is 1.58, which is taken as 1.6 in the study.

$$m = \frac{1}{\sqrt{1 - f_{swmin}/f_{swmax}}} \text{----------(4)}$$

$$L_f = \frac{mV_m}{4h_1 f_{\text{swmax}}} \quad \text{----------(5)}$$

Where

$$h_1 = \sqrt{\frac{k_1}{k_2}\frac{(2m^2-1)}{4m^2} f_{\text{swmax}}} \quad \text{----------(6)}$$

where, $h1$ is the hysteresis band limit, $k1$ and $k2$ are proportionality constants.

B. Design of Series Active Filter VSI Parameters

To design the series active filter system a first-order system, a resistor is added in series with the filter capacitor, referred as switching band resistor (Rsw) [32]. The rms value of the capacitor current can be expressed as

$$I_{\text{se}} = \sqrt{I_{\text{inv}}^2 - I_l^2} \quad \text{----------(7)}$$

Iinv is the series inverter current rating and Il is the load current. The capacitor branch current is divided into two components i.e. a fundamental current Ise1, corresponding to the fundamental reference voltage (Vref1) and a switching frequency current Isw, corresponding to the band voltage (Vsw). The DVR voltage and the current of the capacitor are given by

$$V_{dvr} = \sqrt{V_{ref1}^2 + V_{\text{sw}}^2}$$
$$I_{\text{se}} = \sqrt{I_{\text{se1}}^2 + I_{\text{sw}}^2}$$
$$V_{\text{sw}} = I_{\text{sw}} R_{\text{sw}} = \frac{h_2}{\sqrt{3}}$$
$$V_{\text{ref1}} = I_{\text{se1}} X_{\text{se1}} = \frac{I_{\text{se1}}}{2\pi f_1 C_{\text{se}}} \quad \text{-----(8)}$$

where h2 is the hysteresis band voltage.

The resistance (Rsw) and the capacitance (Cse) values are expressed in terms of band voltage $v$sw and rated references voltage (Vref1), respectively, and are given by

$$R_{\text{sw}} = \frac{h_2}{I_{\text{sw}}\sqrt{3}}$$
$$C_{\text{se}} = \frac{I_{\text{se1}}}{V_{\text{ref1}} 2\pi f_1} \quad \text{----------(9)}$$

The interfacing inductor Lse has been designed based on the switching frequency of the series active filter and is given by

$$L_{\text{se}} = \frac{(V_{\text{bus}})R_{\text{sw}}}{4 f_{\text{swmax}} h_2} \quad \text{----------(10)}$$

where Vbus is the total dc-link voltage across both the dc-link capacitors.

TABLE I
SYSTEM PARAMETERS

System Quantities	Values
System voltages	230 V (line to neutral), 50 Hz
Feeder impedance	$Z_s = 1 + j3.141\ \Omega$
Linear Load	$Z_{la} = 34 + j47.5\ \Omega$, $Z_{lb} = 81 + j39.6\ \Omega$, $Z_{lc} = 31.5 + j70.9\ \Omega$
Non-linear Load	three-phase full bridge rectifier load feeding a R-L load of 150 Ω-300 mH
Shunt VSI parameters	C_{dc} = 2200 μF, L_f = 26 mH, R_f = 1 Ω $V_{dbus} = 2 \times V_{dc}$ = 1040 V (Conventional), V_{dbus} = 560 V(Proposed)
Series VSI parameters	C_{se}=80 μF, L_{se}= 5 mH R_{sw} = 1.5 Ω
Series interfacing transformer	1:1, 100 V and 700 VA
PI controller gains	$K_p = 6$, $K_i = 5.5$
Hysteresis band	$h_1 = \pm 0.5$ A, $h_2 = \pm 6.9$ V

Table I gives specifications for all the parameters.

C. Design of Cf for the Proposed VSI Topology

The design of the *Cf* depends upon the value to which the dc-link voltage is reduced. Most of the electrical loads are combination of the linear inductive and nonlinear loads. Under these conditions, the proposed topology will work efficiently. The design of the value of *Cf* is carried out at the maximum load current, i.e., with the minimum load impedance to ensure that the designed *Cf* will perform satisfactorily at all other loading conditions. If *S*max is the maximum kVA rating of a system and *V*base is the base voltage of the system, then the minimum impedance in the system is given as

$$Z_{\min} = \frac{V_{\text{base}}^2}{S_{\max}} = |R_l + jX_l| \quad \text{----------(11)}$$

To achieve the unity power factor, the shunt active filter current needs to supply the required reactive component of the load current, i.e., the fundamental imaginary part of the filter current should be equal to the imaginary part of the load current. The filter current and load current in a particular phase are given below.

$$\boldsymbol{I}_{\text{filter}} = \frac{V_{\text{inv1}} - V_{l1}}{R_f + j(X_{lf} - X_{cf})}$$

$$\boldsymbol{I}_{\text{load}} = \frac{V_{l1}}{R_l + jX_l} \quad \text{----------(11)}$$

By neglecting the interfacing resistance and equating the imaginary parts of the the above equations results into

$$\frac{V_{l1}X_l}{R_l^2 + X_l^2} = \frac{V_{\text{inv1}} - V_{l1}}{(X_{lf} - X_{cf})^2}(X_{lf} - X_{cf}) \quad \text{----------(12)}$$

From the system parameters mentioned in Table I, phase-*a* load impedance is chosen as *Z*min. The dc bus voltage is chosen to be 560 V for the modified topology, such that it matches with the dc-link voltage requirement of the series active filter (peak of the line to line voltage). Using (12), the value of the the capacitor (*Cf*) is obtained to be 65 μF.

4. GENERATION OF REFERENCE COMPENSATOR CURRENTS UNDER UNBALANCED AND DISTORTED VOLTAGES

When load currents are unbalanced and distorted, these currents flow through the feeder impedance and make the voltage at terminal unbalanced and distorted. The series active filter makes the voltages at PCC balanced and sinusoidal. But the voltages still contain switching frequency componentsand they contain some distortions. If these terminal voltages are used for generating the shunt filter current references, the shunt algorithm results in erroneous compensation [35]. To remove this limitation of the

algorithm, fundamental positive sequence voltages $v^+la1(t)$, $v^+lb1(t)$, and $v^+lc1(t)$ of the PCC voltages are extracted and are used in control algorithm for shunt active filter. In this equation, *Pl*avg is the average load power, *P*loss denotes the switching losses and ohmic losses in actual compensator, and it is generated using a capacitor voltage PI controller. The term *Pl*avg is obtained using a moving average filter of one cycle window of time *T* in seconds. The term ϕ is the desired phase angle between the source voltage and current.

$$i_{fa}^{*}=i_{la}-i_{sa}^{*}=i_{la}-\frac{v_{la1}^{+}+\gamma\left(v_{lb1}^{+}-v_{lc1}^{+}\right)}{\Delta_1^{+}}\left(P_{lavg}+P_{loss}\right)$$

$$i_{fb}^{*}=i_{lb}-i_{sb}^{*}=i_{lb}-\frac{v_{lb1}^{+}+\gamma\left(v_{lc1}^{+}-v_{la1}^{+}\right)}{\Delta_1^{+}}\left(P_{lavg}+P_{loss}\right)$$

$$i_{fc}^{*}=i_{lc}-i_{sc}^{*}=i_{lc}-\frac{v_{lc1}^{+}+\gamma\left(v_{la1}^{+}-v_{lb1}^{+}\right)}{\Delta_1^{+}}\left(P_{lavg}+P_{loss}\right)$$ --(13)

where.

$$\Delta=\sum_{j=a,b,c}\left(v_{lj1}^{+}\right)^2,\gamma=\tan\varphi/\sqrt{3}$$

The above algorithm gives balanced source currents after compensation even if there is unbalanced and distorted supply.

The reference voltages for series active filter are given as

$$v_{\mathrm{dvr}i}^{*}=v_{li}^{*}-v_{ti}$$
$$i=a,b,c$$ ----------(14)

where *v*li* represents the desired load voltages in three phases, and $v^{*}dvri$ represents the reference series active filter voltages.

Once the reference quantities and the actual quantities are obtained from the measurements, the switching commands for the VSI switches are generated using hysteresis band current control method. Hysteresis current controller scheme is based on a feedback loop, generally with two-level comparators.

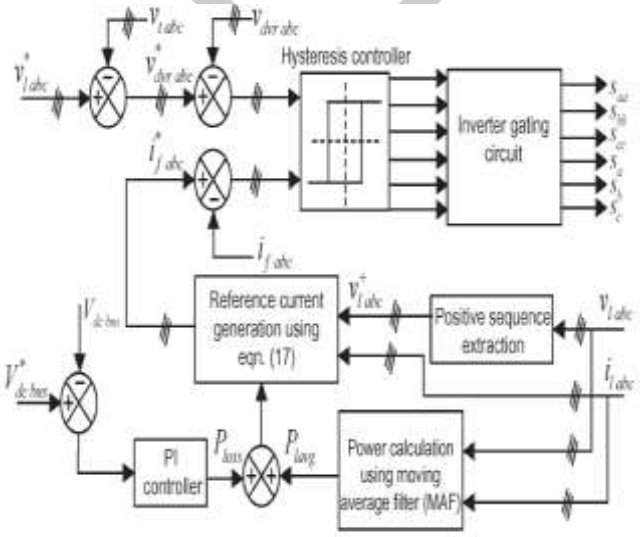

Fig. 3. Control block diagram for UPQC

The switching commands are issued whenever the error limit exceeds a specified tolerance band "±*h*." Unlike the predictive controllers, the hysteresis controller has the advantage of peak current limiting capacity apart from other merits such as extremely good dynamic performance, simplicity in implementation and independence from load parameter variations. The disadvantage with this hysteresis method is that the converterswitching frequency is highly dependent on the ac voltage and varies with it. The switching control law for shunt active filter is given as follows.

5. SIMULATION RESULTS

The simulation results without compensation and with proposed modified topology are presented in this section for better understanding the performance of proposed topology

5.1 Simulation Results without Compensation

The load currents and terminal (PCC) voltages before compensation are shown in Fig. 4. The load currents are unbalanced and distorted as shown in Fig. 4(a), the terminal voltages are also unbalanced and distorted because these load currents flow through the feeder impedance in the system as shown in Fig. 4(b).

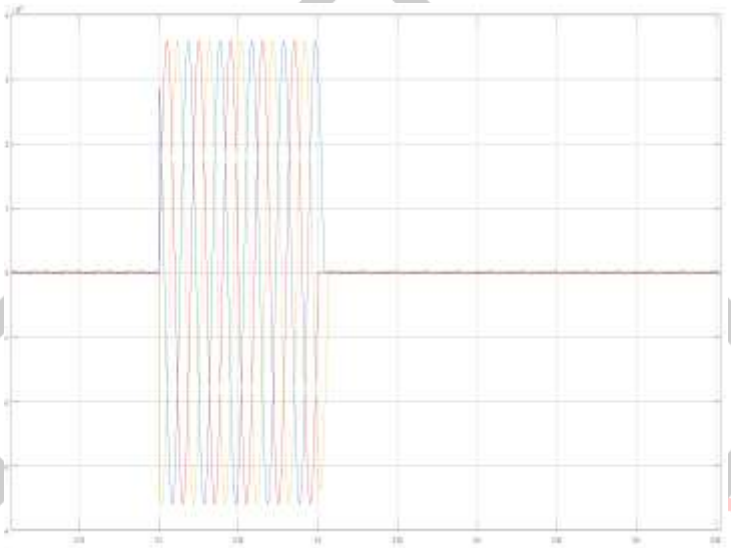

Fig.4 Load current before compensation

The load current before compensation is as shown in Fig4. It can be seen that the load current before compensation is totally distorted. Its magnitude is high than normal current because of harmonic distortions occur due to nonlinear load. Due to harmonic distortions, voltage gets reduced and current gets increased.

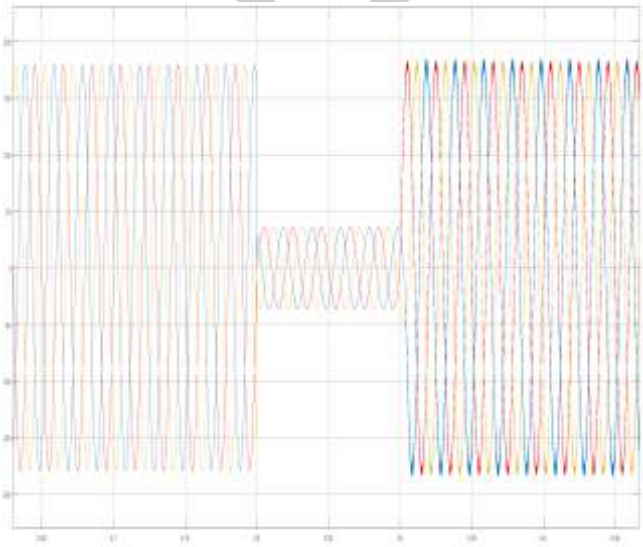

Fig.5 Terminal Voltage before compensation

Terminal voltage before compensation is as shown in Fig.5. It drops to lower value due to harmonic distortions created by nonlinear load.

5.2 Simulation Results with Conventional Topology

To validate the proposed topology, simulation is carried out using MATLAB 2016a software. The same system parameters which are given in Table I with additional Cffor a desired dc-link voltage are used to carry out simulation studies. Fig. 5 gives the simulation results of the UPQC using conventional VSI topology. Using PI controller, the voltage across both dc capacitors are maintained constant as shown in the figure. The source currents after compensation are balanced and sinusoidal as shown in Fig. 6. Fig 7 represents the compensation performance of the series active filter. A sag of 50% is considered in all phases of the terminal voltages for five cycles, which start from 1.9 s and ends at 2.0 s. The compensated DVR voltages and load voltages after compensation are shown in the same figure. The load voltages are maintained to the desired voltage using series active filter.

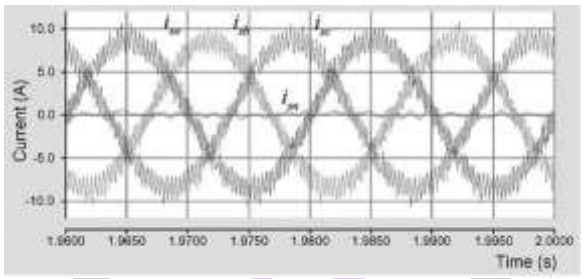

Fig.6 Source Current with Conventional Topology

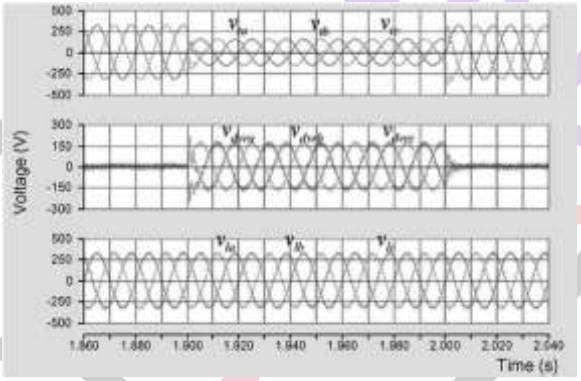

Fig.7 Terminal Voltages with Conventional Topology

5.2 Simulation Results with Proposed Topology

The simulation results with the modified topology are shown in Figs. 8 and 9. In this topology, the value of the capacitor (Cf) in the shunt active filter branch is chosen to be 65 µF, and total dc bus voltage is maintained at 560 V. The voltage across the series capacitor in phase-a (vcfa) and the phase-a load voltage (vla) are shown in Fig. 8. From this figure, it is clear that the voltage across the capacitor is in phase opposition to the terminal voltage. The voltage across the capacitor adds to the dc-link voltage and injects the required compensation currents into the PCC.

The source currents after compensation using modified topology are shown in Fig. 8. The load voltages are maintained to the desired voltage using series active filter. As the voltage across inductor is high in case of conventional topology, the rate of rise of filter current dif/dt will be higher than that of modified topology. This will allow the filter current to hit the hysteresis boundaries at a faster rate and increases the switching, whereas in modified topology, the number of switchings will be less. Thus, the average switching frequency of the switches in the proposed topology will be less as compared to conventional topology.

Since the average switching is less, the switching loss will also decrease in modified topology. A sag of 50% is considered in all phases of the the terminal voltages for five cycles, which start from 1.9 s and ends at 2.0 s. The compensated DVR voltages and load voltages after compensation are shown in the Fig. 9. One more advantage of having less voltage across the inductor is that the hysteresis band violation will be less. This will improve the quality of compensation, and total harmonic distortion (THD) reduces in the proposed topology. Similarly, the switching in the series active filter also reduces marginally as the dc-link voltage

is reduced. This clearly shows the modified topology performance is better than the conventional topology with a less dc-link voltage, reduction in switching operation, and regular tracking of reference compensator currents.

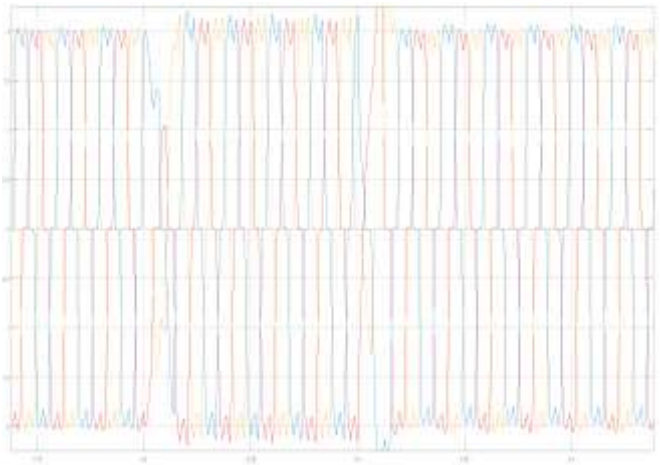

Fig.8 Source current after compensation

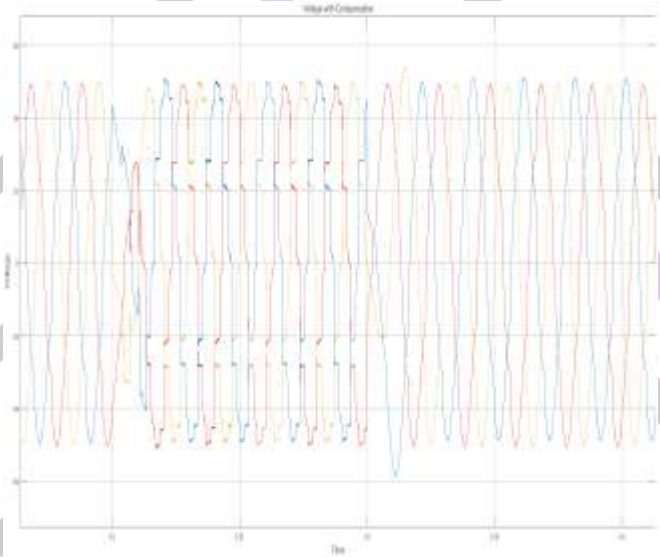

Fig.9 Terminal Voltage after compensation

CONCLUSION

A modified UPQC topology for three-phase four-wire system has been proposed in this paper, which has the capability to compensate the load at a lower dc-link voltage under non-stiff source. Design of the filter parameters for the series and shunt active filters is explained in detail. The proposed modified topology givesthe advantages of both the conventional neutral-clampedtopology and the four-leg topology. Detailed comparative studies are made for the conventional and modified topologies. From the study, it is found that the modified topology has less average switching frequency, less THDs in the source currents, and load voltages with reduced dc-link voltage as compared to the conventional UPQC topology.

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