A Review on UPQC Topologies for Power Quality Improvement

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Abstract: Unified Power Quality Conditioner is a versatile custom power device which mitigates voltage and current related Power Quality issues in distribution system. Modified UPQC topology dealt in this which uses a common DC link voltage for both series and shunt active filter, thus overcoming the need for capacitor voltage balancing in conventional UPQC topology. In some topology, interfacing inductor of shunt active filter is connected in series with a capacitor. The fourth leg of the VSI is connected to negative terminal of DC link and thus eliminates the requirement of fourth leg of VSI. Some topology facilitates UPQC device to have a reduced dc-link voltage without reducing its compensation capability. Some technique constructs by DVR, DSTATCOM, cascaded multilevel inverter and DC-link capacitor.

Keywords: Power Quality, APF, Distribution Static Compensator (DSTATCOM), Dynamic Voltage Restorer (DVR), Reactive Power Compensation, Unified Power Quality Conditioner (UPQC)

1. INTRODUCTION

Present days, power quality problems are the major concerns for the consumers and to the industrial sectors. Power quality problems are mainly because of the power semiconductor devices and the electronic controllers which are used in industries are very sensitive to voltage quality. With the poor voltage quality, harmonics of the system increases and leads to the poor power quality. The different power quality mitigation techniques like SVC, STATCOM, TCSC and UPQC comes under the FACTS controllers mainly designed for enhancing the power quality improvement and reliability. Devices like DVR, DSTATCOM and UPQC etc are mainly used for improving power quality of voltage and current. Among all the devices UPQC gives the best results for the power quality. This is the combination of both the series and shunt active filters. Series active filter (DVR) is connected to source side, mainly reduces the load voltage harmonics and eliminates the supply voltage imbalances. Shunt active filter (DSTATCOM) which is connected to the load side, reduces the source current harmonics and compensates the load reactive power. Configuration of UPQC needs two inverters side by side. UPQC solves the source current and load voltage imperfections. The structure of UPQC shown in Fig.1

The interfacing inductor of the shunt active filter is connected in series with the capacitor (Cf). The series capacitor will enables us in the reduction in DC-link voltage requirement of the shunt active filter and simultaneously it compensates the reactive power required by the load in the system, which will maintain a unity power factor in the system, without compromising the performance of the series capacitor. This will allows us to match the DC-link voltage requirements of both series and shunt active filters in the UPQC device with a common DC-link capacitor.

Unified PQ conditioner (UPQC) is used to protect the electrical and electronic goods which consist of series & shunt inverters connected back-to-back in transmission line and deals with unbalance of voltage & current. Simultaneously UPQC can act...
as shunt and series active power filters. The series active filter of UPQC is called as dynamic voltage restorer (DVR). It can maintain the output voltage constant to the load deviation. The shunt active filter of UPQC is called as distribution static compensator (DSTATCOM), and it is used to compensate load reactive power. The voltage and current phase difference is nil means it make unit power factor. Voltage rating of dc-link capacitor largely influences the compensation performance of an active filter.

2. POWER QUALITY IMPROVEMENT OF THREE PHASE FOUR WIRE SYSTEM USING MODIFIED UPQC TOPOLOGY

In this topology, interfacing inductor of shunt active filter is connected in series with a capacitor. The fourth leg of the VSI is connected to negative terminal of DC link and thus eliminates the requirement of fourth leg of VSI. Switching signals are generated using hysteresis band current controller and Icos $\phi$ algorithm for the operation of UPQC. The performance of modified UPQC topology with hysteresis band current controller and Icos $\phi$ algorithm has been analyzed and comparison has been done using Matlab/simulink.

2.1 MODIFIED UPQC TOPOLOGY

Fig 2 shows the power circuit of the VSI topology for UPQC compensated system. In this figure, the source voltages of phases a, b, and c are termed as $V_{Sa}$, $V_{Sb}$, and $V_{Sc}$ respectively. The source terminal voltages are $V_{Ta}$, $V_{Tb}$ and $V_{Tc}$. The injected voltages of the series active filter are $V_{dvra}$, $V_{dvrb}$ and $V_{dvrc}$ respectively. The three phase source currents are represented as $i_{sa}$, $i_{sb}$ and $i_{sc}$ and the load currents are $i_{la}$, $i_{lb}$ and $i_{lc}$. The shunt active filter currents are denoted as $i_{fa}$, $i_{fb}$ and $i_{fc}$. $L_s$ and $R_s$ are the source inductance and impedance. $L_f$ and $R_f$ are the filter parameters of the shunt active filter. $L_{se}$ and $R_{se}$ are filter parameters of the series active filter respectively. The load used here is shown as unbalanced linear load and non linear loads[1].

Modified UPQC topology has single capacitor in DC link when compared to conventional UPQC which has two DC storage devices in DC link. In conventional UPQC topology series and shunt inverters are controlled independently. Modified UPQC topology are more preferred that conventional because of reduced DC storage device even though it has advantages like smooth tracking with less number of switches. In the modified topology, neutral wire has been connected to negative edge of dc bus, in addition to that capacitor $C$ is connected in series with the inductor of the shunt active filter. The capacitor connected in series, supplies the part of reactive power required by the load and active filter will compensates the balance reactive power and the harmonics present in the load. This topology avoids the over ratings of the series active filter of the UPQC compensation system and also avoids the need of balancing the dc link voltages.
2.2 CONTROLLER STRATEGIES OF UPQC

In this method following controller strategies of UPQC are used.

2.2.1 Hysteresis Band Current Controller

The sensed actual and reference values calculated from the measurements. Switching pulses are generated by Hysteresis band current controller is a two level comparator, based on feedback loop which generates the switching commands for the VSI switches and these switching commands are generated, whenever error value increases to particular tolerance band limit.

2.2.2. Icos \( \phi \) Algorithm

A) Reference Voltage Generation for Series Active Filter

The series active filter control algorithm is given in Fig 4. To synchronize with the supply voltages, a PLL (Phase Locked Loop) is used for the distorted source voltages. The distorted source voltages are given to PLL and it evaluates the 2 quadrature unit matrices (i.e. \( \sin \omega t \) & \( \cos \omega t \))[1].
B) Reference Current Generation of Shunt APF

The shunt active filter control algorithm is given in Fig 5. For the shunt active filter, the fundamental load current component of current is extracted at the zero crossing of the source voltages which are in phase with each other. The source voltages are shifted by 90 degrees using a set of low pass filters. The cut off frequency of these low pass filter is maintained at 50Hz. The sample and hold circuits and zero cross detectors are used to extract the Icos \( \phi \) component from the load current at PCC. The obtained reference source currents are compared with the actual source currents and then given to hysteresis controller and switching signals are generated. Generated switching signal are given to the six switches of Shunt Active Filter.

![Diagram of Shunt active filter controller](image)

**Figure 5. Shunt active filter controller**

3. PHASE 4-WIRE UPQC TOPOLOGY WITH REDUCED DC-LINK VOLTAGE RATING FOR POWER QUALITY IMPROVEMENT USING FUZZY CONTROLLER

3.1 SYSTEM CONFIGURATION

The system under consideration for three-phase, four wire distribution system is shown in Figure 2. The connection of UPQC is made before the load to make the source and the load voltage free from any disturbances. At the same time, the reactive current drawn from the source at source side would be in phase with utility voltages. Supply is made to realize that the voltage harmonics in the source voltage by switching on/off the three-phase diode bridge rectifier. The UPQC, carried on by using two VSIs, is shown in Figure 3: one VSI acts as the series APF and the other as the shunt APF. The shunt APF is performed by using a three-phase, four-leg VSI, and the series APF is carried on by using a three-phase, three-leg VSI. Both APFs are shares a common dc link between them. The four-leg, VSI based shunt active filter is having a capability of load balancing, mitigating the harmonics in the source currents, power-factor correction and negative sequence of the source current[2].
3.2 FUZZY CONTROLLER

The internal structure of the control circuit of fuzzy is shown in Figure 7. The control scheme will consist of limiter, Fuzzy controller, and three phase sine wave generator which generates reference current and switching signals. The peak value of reference currents will be estimated by regulating the DC link voltage. The actual capacitor voltage will be compared with a set of reference values. The error signal is then processed over a Fuzzy controller, which contributes to zero steady error in tracking the reference current signal.

A fuzzy controller will convert a linguistic control strategy into an automatic control strategy, and fuzzy rules are constructed by expert or experience in knowledge database. Firstly, the input reference voltage Vdc-ref and the input voltage Vdc have been placed of the angular velocity to be the input variables of the fuzzy logic controller. Then the output variable of the fuzzy logic controller will be presented by the control Current Imax. To convert these numerical variables into linguistic variables, the following seven fuzzy levels or sets are chosen as: ZE (zero), PS (positive small), PM (positive medium), PB (positive big) NB (negative big), NM (negative medium), and NS (negative small).

This UPQC topology having the capability to compensate the voltage swells, voltage sags and current harmonics at the load at a lower DC-link voltage by using different control strategies for series and shunt APF’s.
4. THREE-PHASE 3-WIRE VOLTAGE SOURCE INVERTER BASED UPQC

4.1 CONFIGURATION OF UPQC BY SIMULTANEOUS CONTROL OF DVR AND DSTATCOM

The main purpose of a UPQC is to compensate for supply voltage flicker/imbalance, reactive power, negative-sequence current, and harmonics. In case of sag and swell in the power system, Dynamic Voltage Restorer (DVR) provides series compensation by voltage injection. The Distribution Static Compensator (D-STATCOM) provides continuously variable shunt compensation by current injection. This eliminates fluctuations in voltage. Unified Power Quality Conditioner (UPQC) eliminates the harmonics in the supply current improves utility current quality for nonlinear loads. UPQC provides the VAR requirement of the load, so that the supply voltage and current are always in phase eliminating the necessity of additional power factor correction equipment. UPQC maintains load end voltage at the rated value even in the presence of supply voltage variations. The UPQC consists of two three phase inverters which are series and shunt inverters connected in cascade. The series inverter is connected in series with the supply voltage through a transformer. The shunt inverter is connected in parallel with the load. The main purpose of the shunt compensator is to compensate for the reactive power demanded by the load, to eliminate the harmonics and for regulation of common dc link voltage. The series compensator is operated in PWM voltage controlled mode. It injects voltage in quadrature advance to the supply voltage (current) such that the load end voltage is always maintained at the desired value. The two inverters operate in a coordinated manner. The operation of a UPQC that combines the operations of a Distribution Static Compensator (D-STATCOM) and Dynamic Voltage Restorer (DVR) together[3].

In this topology, the Phase Locked Loop (PLL) system can be used to synchronize on a set of variable frequency, three-phase sinusoidal signals. Discrete Pulse Width Modulation (PWM) Generator generates pulses for Carrier based Pulse Width Modulation. The carrier frequency of the switching devices is 12000 Hz. The generator mode is taken as a 3-arm bridge (6 pulses). The common DC-link capacitor has a capacitance of 5000μF with an initial voltage of 600V across it. The Discrete ProportionalIntegral (PI) Controller is in series with the active filter. Control of series part of UPQC is based on discrete PI Controller and control of shunt part of UPQC is based on discrete PLL and discrete PWM Generator. In order to validate the performance of 3P 3W VSI based UPQC, the block diagram configuration shown in Fig.4 is simulated in Matlab/ Simulink environment. The primary condition for reactive power compensation is that the magnitude of reference dc-bus capacitor voltage should be higher than the peak voltage at the point of common coupling (PCC).

The source currents after compensation are balanced and sinusoidal. The unbalanced and distorted load voltages are maintained to the desired voltage using series active filter. The shunt filter currents which are injected into the point of common coupling to make the source currents balanced and sinusoidal. The simultaneous performance of the shunt and series active filter of the UPQC is studied by compensating the load current and maintaining the load voltage to the desired value during any changes in voltage. The load voltages after compensation are balanced and sinusoidal.
5. THREE-PHASE 4-WIRE UPQC TOPOLOGY WITH REDUCED DC-LINK VOLTAGE RATING

The proposed topology enables UPQC to have a reduced dc-link voltage without compromising its compensation capability. This proposed topology also helps to match the dc-link voltage requirement of the shunt and series active filters of the UPQC. The topology uses a capacitor in series with the interfacing inductor of the shunt active filter, and the system neutral is connected to the negative terminal of the dc-link voltage to avoid the requirement of the fourth leg in the voltage source inverter (VSI) of the shunt active filter. The average switching frequency of the switches in the VSI also reduces, consequently the switching losses in the inverters reduce[4].

![Fig.9  Equivalent Circuit of 3-Phase 4-Wire UPQC Topology with Reduced DC-Link Voltage Rating](image)

In this topology, the system neutral has been connected to the negative terminal of the dc bus along with the capacitor Cf in series with the interfacing inductance of the shunt active filter. This topology is referred to as modified topology. The passive capacitor Cf has the capability to supply a part of the reactive power required by the load, and the active filter will compensate the balance reactive power and the harmonics present in the load. The addition of capacitor in series with the interfacing inductor of the shunt active filter will significantly reduce the dc-link voltage requirement and consequently reduces the average switching frequency of the switches. This concept will be illustrated with analytic description in the following section. The reduction in the dc-link voltage requirement of the shunt active filter enables to match the dc-link voltage requirement with the series active filter. This topology avoids the over rating of the series active filter of the UPQC compensation system. The design of the series capacitor Cf and the other VSI parameters have significant effect on the performance of the compensator. This topology uses a single dc capacitor unlike the neutral-clamped topology and consequently avoids the need of balancing the dc-link voltages. Each leg of the inverter can be controlled independently in shunt active filter. This topology has the capability to compensate the load at a lower dc-link voltage under no stiff source.

6. RESULTS AND DISCUSSION

A 3-phase 4 wire UPQC topology using series and shunt active filter uses a common dc-link having appropriate voltage which is suitable to both series and shunt active filter. This topology uses a single dc capacitor unlike the neutral-clamped topology and consequently avoids the need of balancing the dc-link voltages. Each leg of the inverter can be controlled independently in shunt active filter. This topology has the capability to compensate the load at a lower dc-link voltage under no stiff source. This topology gives advantages of both the conventional and neutral clamped topology and four leg topology.

References


