Review: Hybrid PLL for Controlling Master-Slave Configured Centralized Inverters with three-phase single-stage grid tied solar photovoltaic energy conversion system using phase locked loop

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***Abstract* – This paper The main intent of this paper is to integrate a SPV generating system to three-phase grid and to provide a clean and uninterrupted flow of power at abnormal and peak load conditions and also proposed a HPLL algorithm for high power MSC centralized inverters for large Photovoltaic (PV) power plants. This paper presents a three-phase single-stage grid tied SPECS using phase locked loop-less (PLL-less). This system uses a single-stage perturb & observe (P&O) approach for maximum power point tracking (MPPT). The proposed PLL technique along with the existing techniques is simulated and compared in MATLAB/SIMULINK and digitally implemented in TMS320F2812 based Discrete Signal Controller (DSC). The performance of the proposed HPLL technique is experimentally validated with unbalanced and distorted grid signals. Experimental results of proposed HPLL show faster grid synchronization in MSC based grid-connected inverter, LVRT capability and dynamic interleaving of MSC inverters.**

***Keywords*: Phase Locked Loop (PLL), Hybrid PLL, Master-slave based centralized inverter, Synchronous reference frame, VSI**

I. INTRODUCTION

Photovoltaic cells and modules have shown great promise in the field of efficient solar energy conversion technologies. Solar photovoltaic (SPV) technology is widely considered as a sustainable and substantial renewable energy source to counter against climate shifts. The diffusion of SPV energy conversion system (SPECS) to the distribution network contributes to greenhouse gases mitigation, temperature benefits and restrains several other climatic calamities [1].The enhanced penetration of renewable energy sources such as solar photovoltaic (PV) and the wind into the existing power grid has increased the overall percentage of power converters connected to the grid. Today, these converters have become an integral part of our electrical power system. In India as per Jawaharlal Nehru National Solar Mission (JNNSM) phase – II, these high power converters should be in compliance with IEEE/IEC standards. The high power converters [5,6] used in large PV power plants generally employ master-slave scheme. A typical Master Slave Configured (MSC) centralized inverter is shown in Fig. 1 where several inverters are connected in parallel. The MSC inverter offers the following distinct advantages:

(a) Scalability to a higher power.
(b) Better component utilization and relatively long life of the electronic components (i.e. capacitors, switching devices etc.).
(c) Smaller footprint and higher reliability with lower THD levels.
(c) In case of an inverter failure, the total power output doesn't go to zero as other inverters can continue to export partial power into the AC grid.
(d) Smaller footprint and higher reliability with lower THD levels.
(e) Better controllability in the export of power to the grid.

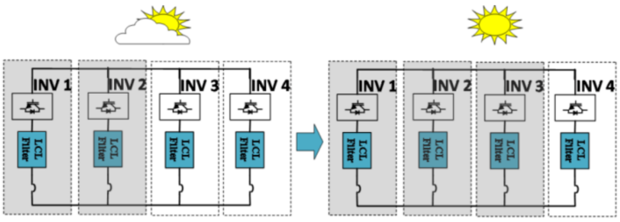


Fig. 1. Master-slave based centralized inverter system for a large PV power plant.

The MSC systems are directly connected to medium voltage grid and it is expected that their performance remains unaffected by grid voltage and frequency variation and should be in compliance with IEEE/IEC standards [2-4] for interfacing power converters to the utility.

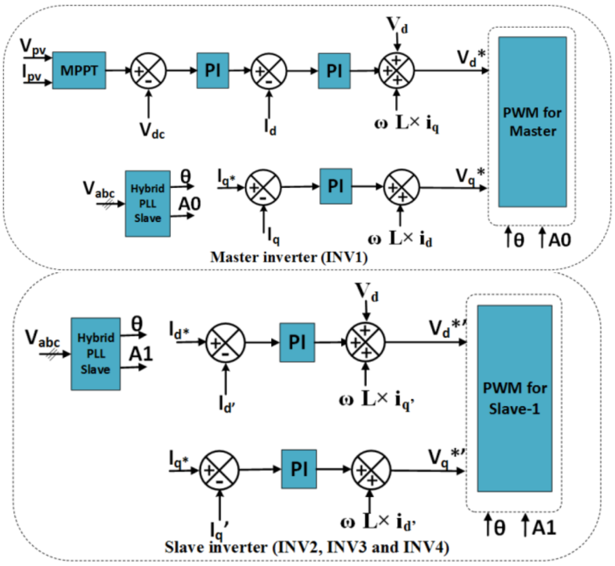


Fig. 2. Block diagram depicting the d-q current control of MSC centralized inverter

The performance of these loops depends on the correct estimation of grid phase and the frequency with the help of a 3-ϕ software PLL, which is embedded in the controller. Hence, the PLL plays a very important role in the correct determination of grid angle and proper functioning of the controller. These 3-ϕ PLLs should not only work with balanced grid voltages but also work properly under unbalanced and distorted grid conditions. PLL for master-slave configured centralized inverter system has to ensure not only the correct estimation of grid phase and frequency but also faster synchronization and dynamic interleaving angle adjustments for reducing the Total Harmonic Distortion (THD) at the PCC.

II. REVIEW OF EXISTING PLL ARCHITECTURE

PLLs are used for determining the phase and frequency of the 3-ϕ grid and this information is used by the controller for controlling currents injected into the grid. There are many PLL schemes which are briefly reviewed in this section.

A. *Basic 3-ϕ Synchronous Reference Frame PLL*

The basic structure of a PLL is shown in Fig. 3. It consists of a phase detector and a loop filter followed by a voltage controlled oscillator (VCO). The PI structure acts as a loop filter and feed-forward term (ωff) along with the integrator acts as a Voltage Control Oscillator [VCO].

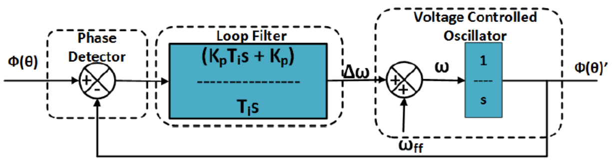


Fig. 3 Linearized model of the basic PLL

The control structure of an SRF PLL [7-10] is shown in Fig. 4. First the 3-ϕ voltage Vabc is transformed to d-q frame as per the following equations, in order to synchronize with the peak of phase voltage (Va), the Q component (Vq) is made zero.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} V_m Cos(\theta) \\ V_m Cos(\theta - 120^\circ) \\ V_m Cos(\theta + 120^\circ) \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 0 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} Cos(\theta') & Sin(\theta') \\ -Sin(\theta') & Cos(\theta') \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (3)$$

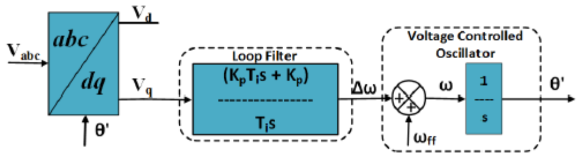


Fig. 4. Block diagram of SRF PLL in the synchronous reference frame.

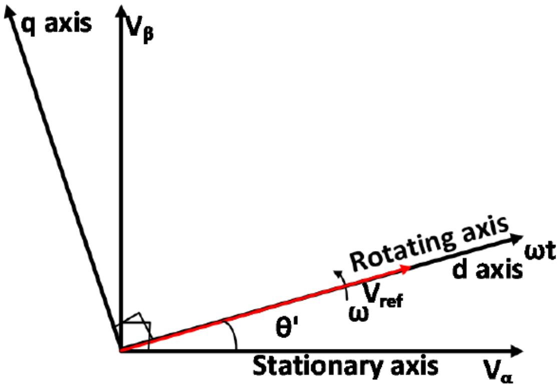


Fig. 5. Stationary reference frame (Vα and Vβ) and rotating reference frame (Vd and Vq).

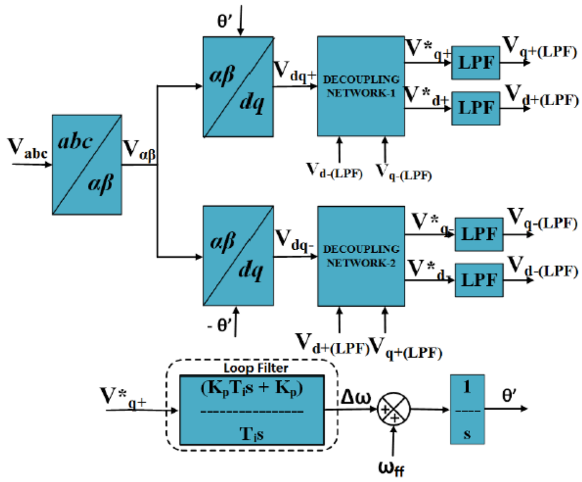


Fig. 6. 3-□ PLL block diagram of DDSRF with two decoupled networks-1/2.

$$\begin{bmatrix} V_{d-}* \\ V_{q-}* \end{bmatrix} = \begin{bmatrix} V_{d-} \\ V_{q-} \end{bmatrix} - \begin{bmatrix} Cos(2\theta') \\ Sin(2\theta') \end{bmatrix} \left[V_{d+(LPF)} \right]$$

….(4)

III. PROPOSED 3-Φ HYBRID PLL

A hybrid PLL architecture [23] is proposed for master slave-based centralized inverter where the center frequency (ωc) is calculated using the 1-ϕ EPLL

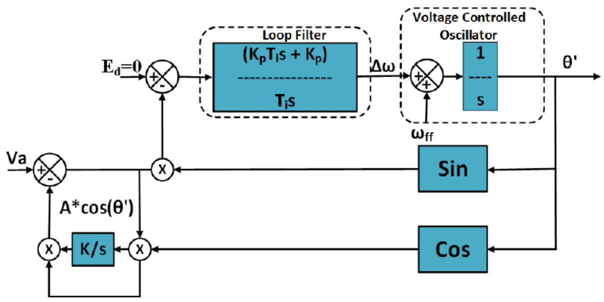


Fig. 9. Block diagram of the 1-Φ EPLL

The equation for error (Ed) is given below; the error (Ed) becomes zero when the output of the EPLL generates a signal whose amplitude, phase and frequency match with the grid signal.

$$Ed = \frac{Vm}{2}Sin(\theta' - \theta) + \frac{Vm}{2}Sin(\theta' + \theta) - \frac{A}{2}Sin(2\theta')$$

..(5)

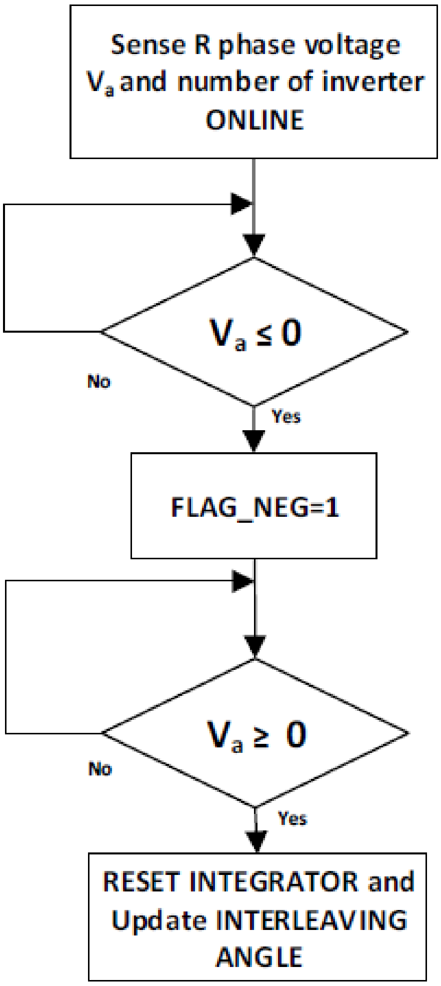


Fig. 10. Flow chart for ZCD of proposed hybrid PLL

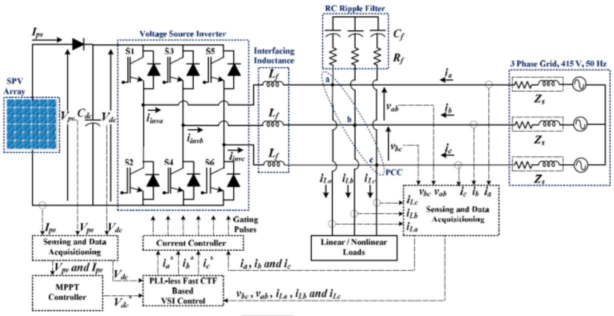
IV. MAXIMUM SYSTEM STRUCTURE OF THREE-PHASE SINGLE-STAGE GRID TIED SOLAR PV ENERGY

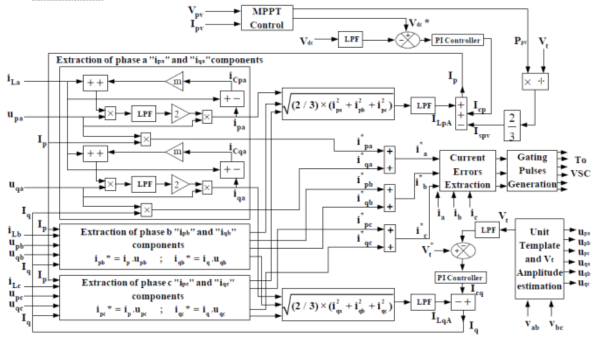
MPPT The presented system incorporates a single-stage SPECS tied to three-phase distribution grid and connected loads (linear and nonlinear) which is depicted in Fig. 1 (a). SPECS is composed of a SPV array, a diode, a DC link capacitor and a VSI (Voltage Source Inverter). Using a diode ensures protection of the SPV array by blocking the reverse power flow from the distribution network. The DC link capacitance reduces the fluctuations in the DC voltage at the input terminals of the VSI. An essential element of the presented system is the VSI which functions as a DC-AC power conversion device for the DC power extracted from the SPV array and converts it into the AC power to be synchronized with the three-phase distribution network. Moreover, other essential components of the presented system include an interfacing .

A. Control Technique

The basic control technique of the presented system involves two major operations. The first step is tracking the MPOP of the SPV array to extract maximum power at changing environmental conditions.
The next step is VSI control which employs the improved character of triangle function (CTF) with phase locked loop-less (PLL-less) method.

1. MPPT Control
Apart from several advantages, the SPV system suffers from low conversion efficiency. Therefore, a variety of MPPT techniques have been discussed in the literature [7-14]. P&O based approach is applied as the MPPT method to enforce the single-stage topology of the presented system. P&O approach is very simple and generic in nature involving a trade-off between its rate of response and the amount of oscillations at the steady state conditions. The output of the MPPT control is considered the reference value of DC link voltage (Vdc*) for the VSI. Some of the approaches of implementing P&O method have been reported in the literature [28-29]. 3.2. PLL-less Fast CTF Control The control architecture of the PLL-less fast CTF control is depicted in Fig. 1 (b). The functions of
this control method are the extraction of fundamental components of load currents, estimation of in-phase and quadrature unit templates, estimation of AC and DC loss components and calculation of the reference grid currents. After that the reference grid currents and sensed grid currents are passed through the current error extractor and the hysteresis regulator to generate the gate signals for switching of the VSI. 3.2.1 Estimation of Unit Templates and Amplitude of Terminal Voltages: From the sensed PCC line voltages (vab and vbc), the phase voltages are obtained from equations in [30] as,





To generate gate pulses for the switching of the VSI, an indirect current control technique is used with a hysteresis current regulator. The error current signal is calculated from the difference between the reference value of grid currents (iabc*) and the sensed grid currents (iabc) which are then passed through the hysteresis current regulator (hysteresis width, $\delta = 0.01$) for generating six gating pulses.

B. Comparison between Conventional CTF Control and PLL-less fast CTF Control

The control diagram of the conventional CTF control is shown in Fig. 1 (c) and proposed PLL-less fast CTF control is shown in Fig. 1 (d). From Fig. 1 (c), it is understood that for the extraction of fundamental component ‘ipa’, phase of voltage ‘vs’ is obtained using PLL block. The detailed equations for conventional CTF control are provided in [27]. Whereas, in proposed PLL-less fast CTF control, instead of using the complex PLL block, the phase of voltage ‘vs’ is obtained via unit template calculation which produces unit vectors from equations (1-4). Moreover, conventional CTF requires RMS (Root Mean Square) block to produce its fundamental signal output but the proposed control does not require this block. The use of complex blocks like PLL and RMS increase the computational time and task for the low-end processors therefore the proposed control has a better computational efficiency. The proposed control has a high DSP speed, low sampling time and good response to changes as compared to the conventional control.

V. SIMULATION RESULTS

The presented system is designed, modelled and simulated in a MATLAB/Simulink environment making use of available simpower system (SPS) toolbox. The design and modelling of a SPV array are done through a procedure reported in the literature [32]. Moreover, the SPECS is designed for a maximum power capacity of 6.8 kW, 290 V and 50 Hz. Likewise, the designing of other essential elements such as DC link voltage and capacitance, interfacing inductance, ripple filter and connected loads are also carried out in detail [31]. A comprehensive set of data is given in Appendices. The behaviour of the presented system is studied under unbalanced nonlinear loads and varying solar intensity at UPF (Unity Power Factor) mode of operation that particular phase voltage in that interval is uncertain if the load is unbalanced.

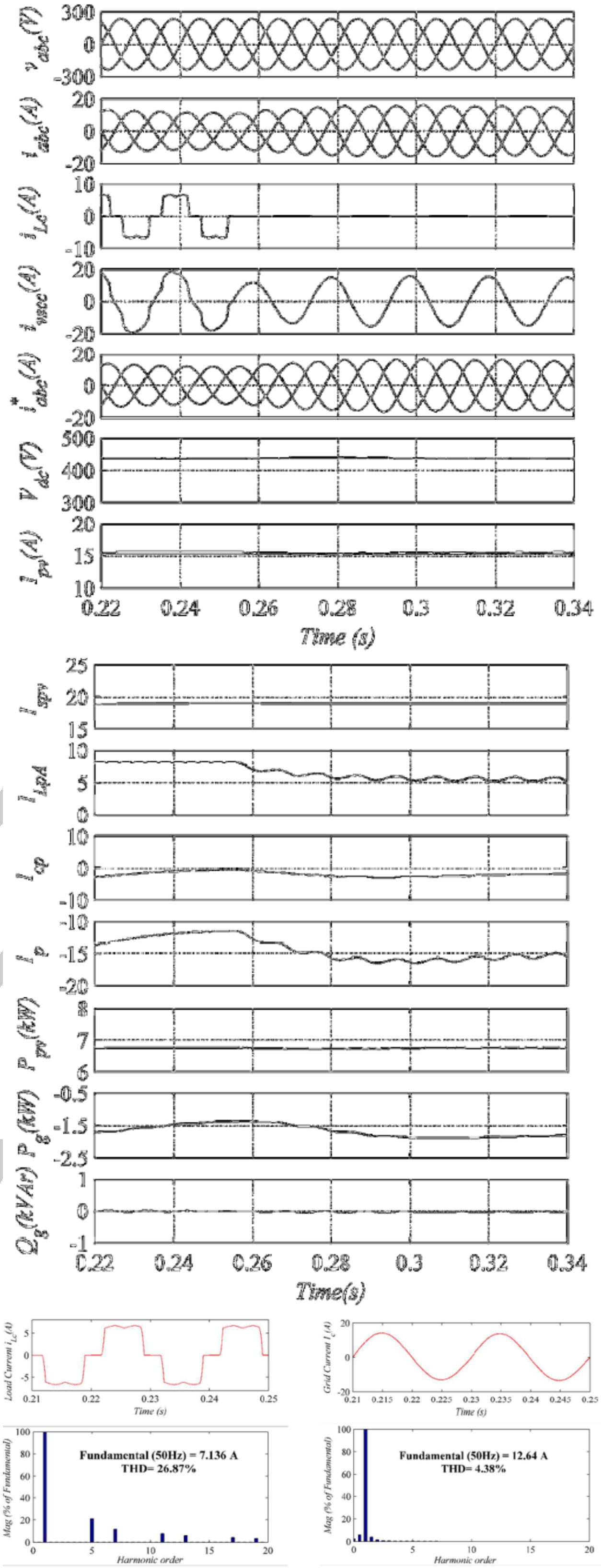


Fig. 11 Dynamic Performance under unbalanced nonlinear load

VI. CONCLUSION

For Hybrid PLL for Controlling:

3-ϕ PLL plays an important role in the correct estimation of grid phase and frequency for the control of grid-connected MSC centralized inverters usually employed in large PV power plants. These 3-ϕ PLLs are expected to work with voltage and frequency variations. Many 3-ϕ PLLs such as SRF, DSOGI with FLL and DDSRF are extensively used in centralized inverters. These PLLs except SRF can work under unbalanced and distorted grid conditions. Proposed Hybrid PLL enables correct estimation of grid phase, frequency, faster synchronization and software interleaving using timer synchronization. Proposed PLL enhances the performance of PV fed master-slave configured centralized inverter systems. Proposed PLL with ZCD enables faster synchronization as shown in Fig. 16(a) during inverter start-up and can be used in high power master-slave based centralized inverters where inverters frequently switch ON/OFF depending on the power availability of PV modules.

For three-phase single-stage grid tied solar photovoltaic energy conversion system using phase locked loop:

A PLL-less fast CTF based control technique has been presented for a three-phase grid tied singlestage SPECS for the extraction of in-phase and quadrature components of load currents. The validation of the model and control has been carried out through simulations done in MATLAB/Simulink using simpower system (SPS) toolbox. Moreover, the experimental verification of the presented system has also been carried out on a prototype in the laboratory. The main advantages of this PLL-less fast CTF control approach are that it is very simple, easy to implement and has a fast response. Simulation results haveshown that the presented grid tied SPECS has performed satisfactorily under unbalanced nonlinear loads
and variable solar intensity

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