BIST Memory Design and Testing

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Abstract: **Memories are the most essential component in all storage devices. Memory structure become complex when it is upgrading. Due to higher level of integration in memory size, manufacturing cost of the device is reducing and testing cost is increasing. Testing is needed to give the fault free products. Large number of bit pattern requires more time to test the circuit. Test algorithms are necessary to minimize the testing time. In this paper memory is designed and tested for stuck at fault with single bit and multiple bit error. We have simulated and analyzed the memory design using Xilinx design suite ISE 14.2.**

Index Terms: **Memory, BIST, LFSR, Test data.**

I.INTRODUCTION

In a silicon die different types of memories can be fabricated and it is called as System on Chip. The advantage of SOC is low power consumption in computing market and it gives the efficient fault coverage for a targeted fault. RAM and ROM are the most common two different types of memories. Almost all memories having the property of random access .Volatile memory losses it stored data when the power to the chip is turned off but it is less expensive than non-volatile memory.

This paper is organized into five sections. Section II explores the related work done by various researchers followed by the presentation of BIST Architecture and faulty algorithm in section III. The experimental results and discussions are presented in section IV. Section V presents conclusion and future scope.

II.LITURATURE SURVEY

2.1 Testability

As SOC contains various functional components, they are predesigned and pre-verified by the core providers. System integrators are provided for verification of the design and manufacturing testing to analyze the complexity of SOC, Testing embedded memory is more difficult than testing commodity memory. The first testing issue is accessibility .When the DRAM core is embedded in a CPU or ASIC and surrounded by logic blocks. Proper Design for Testability (DFT) methodology must be provided for core isolation and tester access, and a price has to be paid for the resulting hardware overhead, performance penalty, and noise and parasitic effects.

2.2. Test data and testing time

Power dissipation becomes a serious concern in memory inputs with memory BIST features due to switching activity in the memory under test, the read &write operation requires a lot of switching in test pattern generator and address counter. Modern Automatic Test Pattern (ATGP) tools tend generate test patterns with a high toggle rate in order to reduce the pattern count .parallel testing is often used to reduce test application time, particularly on (SOC) device.

2.3. Issues of Test power

When verifying the correct function of high –density system such as an SOC, test procedures and test techniques have to satisfy all power constraints in the design phase, otherwise it can expose the circuit to various problems such as, reducing reliability, product cost increase etc. An excessive switching in the CMOS circuit can cause catastrophic problems such as instant circuit damage ,reduced autonomy for device that are operate by battery

2.4. Memory Testing

Memory consists of group of cells. Semiconductor memories are considered as one of the most important aspects of modern VLSI system. Memories are the most universal component in system on chip today. All SOC's contain some types of embedded memories such as RAM, ROM, DRAM and flash memory. Testing the memory and SOC becomes more important because the memory density higher than the logical part. Which means chance to have a defect is higher in memory. The BIST methodologies offer solutions for testability of embedded memories and minimize the embedded memory tester's requirements and reduce memory test time

2.5 Cost Function Evaluation

In order to test the optimality of a solution, a cost function is defined. In this implementation, the cost is defined as the number of used spare elements. The Solver has a register to store the cost of the current repair strategy. The Solver also has registers to store the repair strategy with minimum cost so far and the minimum cost. The current cost is compared against the minimum cost

generated so far. If the cost of current repair strategy is more than minimum cost, the Solver immediately asserts the Restart signal and moves on to the next repair strategy. If the cost of the current repair solution is less than minimum cost till the end of the evaluation, the Solver saves the current repair strategy and its cost.

2.6 Fault models.

A fault model is defined as one in which occurrence of fault and their impact on circuit is analyzed .Which can be done before actual testing. The common faults that may occur in the memory are Stuck at Faults (SAF), Stuck open or Stuck short faults, Address Faults (AF), Coupling Fault (CF), Bridging Fault (BF), Software Fault (SF).When there is high transmission of bit from 1 to 0 result will be 0 instead of 1 this type fault is called Software Fault. If the signal line is permanently fixed to logic zero, it is called Stuck-at Zero and if it is permanently connected to a logic1, it is called Stuck at One fault model.

III. BIST ARCHITECTURE AND MEMORY DESIGN

The external interface in RAM is made of three groups of signals, address signals, control signals and data signals. The control signals tell the RAM what operation is to be executed i.e., Read or Write. The address signals tell the RAM the cell location to perform the operation on and finally the data signals to transfer the data to and from the RAM.
During Write operation, the data is first loaded into the memory. During Read operation, written data is displayed on the data-out line.

3.1. Memory BIST Controller

For detection of faults occurred in memories we use test algorithms. The dominant test algorithms that are currently implemented in Memory BIST Controller March test techniques it is simple and can be used to have good fault coverage.

MBIST Controller features a set of predefined instructions that is used to write the selected test algorithms. The written tests are loaded in the MBIST controller. This type of MBIST the test patterns, data, address and control signals. These test patterns are applied to memory which is under test.

3.2. Built In Self Repair

Memories are the key components in SOC. They are dense and cover a large portion of chip area. There may be a fault occurs when data is transmitted at the high rate. For this concern we have to use rows and/or spare columns and cells –to improve the yield. The defective cells detected by the BIST circuit are replaced by the spare memory.

BISR circuit can only identify faulty chip. It requires the fail address data and spare memory. This method compares the input data with stored data.

3.3 BIRA

It collects the faulty information from the MBIST circuit and allocates the redundancies according to the collected faulty information using the implemented redundancy analysis algorithm. The BIRA unit mainly consists of MBIST block and BIST block which are capable for testing the memory under test as well as perform the Self Repair in the memory address test.

3.4 Solver

The solver will generate the repair strategies one by one and will check whether each repair strategy can fix all the faulty captured in the faulty list. The first repair strategy is generated depending on the number of must repair rows and coloumns. After repair strategy is tested, the state of the MRA should be reverted. The MRA reads the each faulty address in the fault list in order until there is no fault address. MRA will also display which bit is error in the given input data.

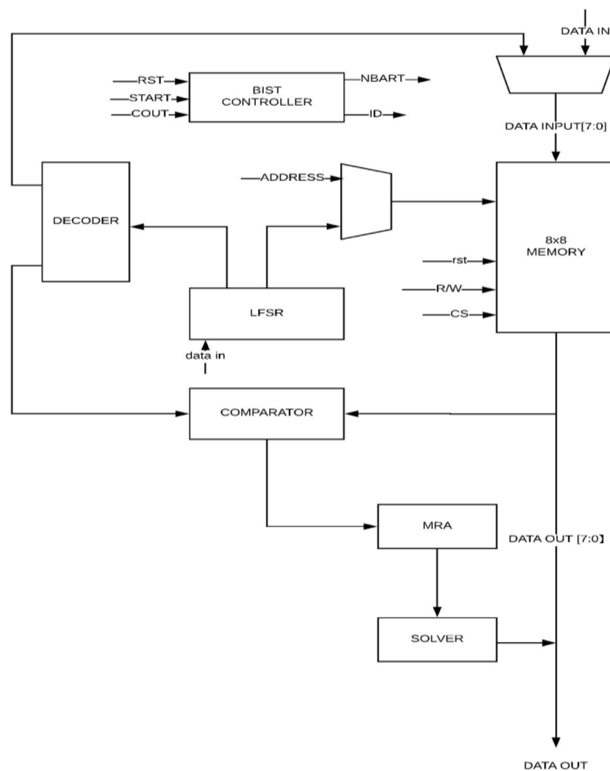

Fig. 3.1 Block Diagram of Memory BIST

IV. RESULTS

Simulation results using Xilinx ISE Design Suite 14.2

Test data generation: In this operation Linear Frequency shift Register is used to generate the test data. By connecting a 8-D flip flop serially with the XOR gate test pattern is generated continuously with counting each clock pulse. LFSR gives the data continuously by enabling the clock and giving 8-bit input data memory as shown in Fig. 4.1.

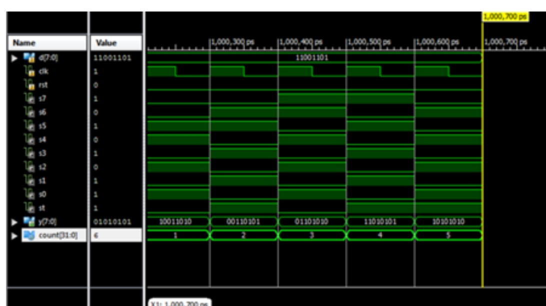

Fig 4.1 Simulation results for LFSR pattern generator

Memory write operation: In this operation 0 to 1 transition of clock signal, reset zero, and enabling write pin high and then giving the data in data is written in to the memory. The design is realized using Xilinx ISE 13.2 as shown in Fig. 4.2.

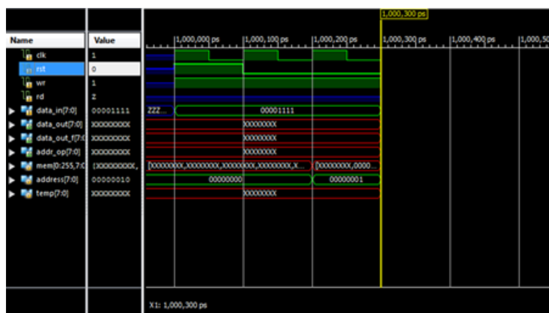

Fig. 4.2 Simulation results for memory WRITE operation

Memory Read operation: In this operation 0 to 1 transition of clock signal, reset zero, disabling the write pin and enabling the read pin high ,then given data is read from the memory as shown in Fig. 4.3.

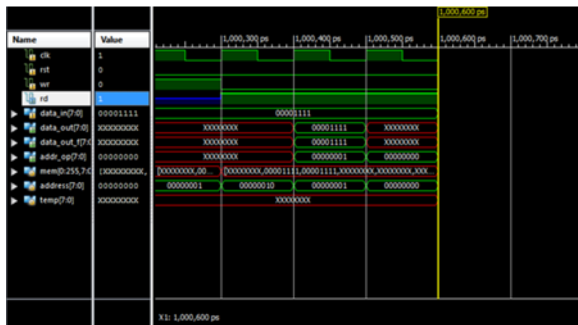

Fig. 4.3 Simulation results for memory READ operation

Fault detection: In this operation fault is injected into different address locations. The faulty data present in the memory is identified and it's address locations were displayed in the output as shown in Fig. 4.4.

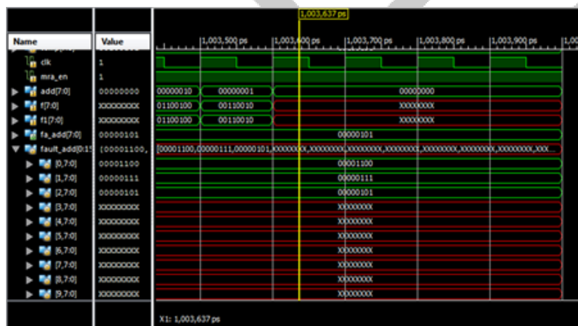

Fig. 4.4.Simulation results for Locating faulty data address

Fault data correction: The faulty data and its address locations were identified. Comparator will gives which bit in the 8-bit input data is error and new data is written as shown in Fig. 4.5.

Fig .4.5 Simulation results for writing a new data

Solver: In this operation spare line are used to write the new data and it gives the output data as shown in fig 4.6.

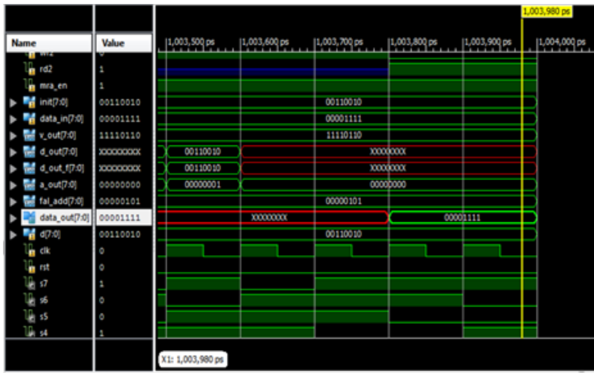

Fig 4.6.Simulation results for final data out

RESULT ANALYSIS TABLE

Single Bit Error

INPUT ADDRESSS LOCATION	ERROR BIT POSITION	AREA IN SLICE LUT'S	DELAY IN ns
00000101	11111110	356 out of 30064	4.404 ns
00001010	11110111		
00001111	01111111		

Two Bit Error

INPUT ADDRESSS LOCATION	ERROR BIT POSITION	AREA IN SLICE LUT'S	DELAY IN Ns
00000101	11111100	80 out of 30064	4.270 ns
00001010	11110011		
00001111	00111111		

Multi Bit Error

INPUT ADDRESSS LOCATION	ERROR BIT POSITION	AREA IN SLICE LUT'S	DELAY IN Ns
00000101	11110000	84 out of 30064	4.384 ns
00001010	10110101		
00001111	01011010		

V. CONCLUSION AND FUTURESCOPE

An efficient Memory architecture has been Presented and memory operations and testing conditions are simulated using Xilinx design suite ISE 13.2.We have Injected and tested the stuck at faults in BIST memory. Different test algorithms can be developed to cover different faults with more fault coverage.

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