

# DESIGN OF A THREE BIT TERNARY PREFIX ADDER USING CNFET

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**Abstract:** Multi-valued logic (MVL) is that logic which has two or more logic values. In complex digital circuits, MVL (mainly Ternary logic) offers several advantages over binary logic. Carbon Nanotube Field Effect Transistor (CNFET) technology is ideal to implement ternary logic circuits because of the threshold voltage of CNFETs depends on the physical dimensions (chirality) of their channel. This work presents the implementation of a three-bit Ternary Prefix Adder using CNFET technology. In this paper, a carry propagate-generate concept is used in order to implement the ternary prefix adder. A Kogge-Stone based prefix network is preferred for carry computation due to its high performance. HSpice tool is chosen for designing this system. Simulation results show that there is a significant reduction in power consumption and propagation delay by 43% and 72% respectively.

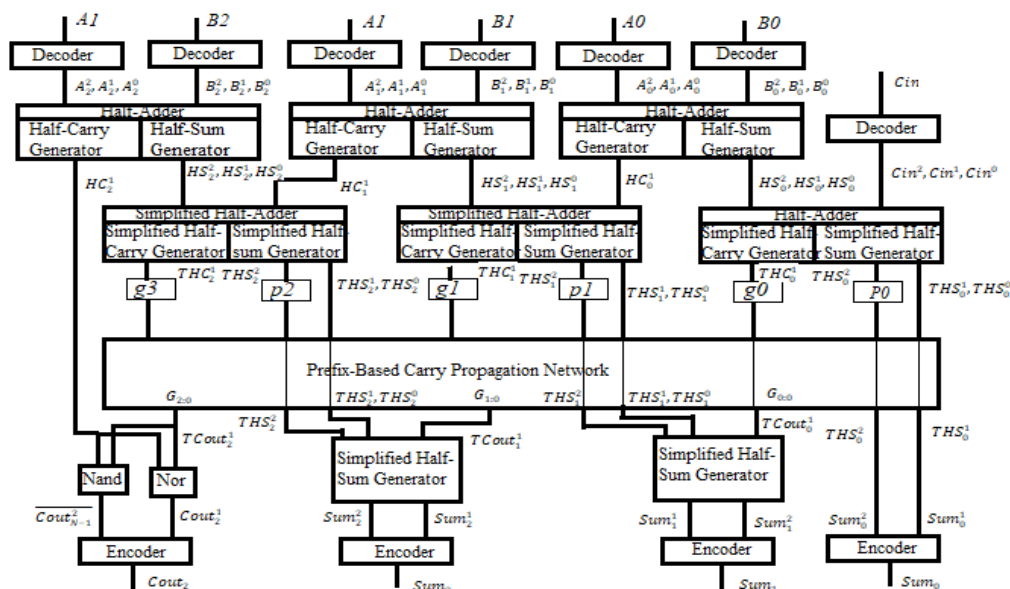
**Index Terms:** CNFET, Prefix Adders, Ternary Logic, Low power

## I. INTRODUCTION

Ternary logic circuits are highly energy efficient and hence are utilized in application emphasizing on reduced complexity of chip area and interconnects. CNFET have replaced MOS transistors in designs requiring high performance in low power consumption. These are preferred in implementing MVL circuits as the desired threshold voltage can be obtained by varying the physical dimensions (diameter). The advantage of using CNFET over CMOS for ternary designs is well described in the literature [1]. One of the first ternary logic circuit approach using CNFET has been presented in [2]. The major limitation of this methodology is the use of resistive loads which leads to large off-chip resistance. A better approach, which uses an active load with p-type instead of large resistances, has been introduced in [4], [5]. The advantage of using pseudo-n-Type CNFETs as an active load has been demonstrated recently in [6]. There have been many implementations of CNFET-based arithmetic circuits (like Comparator [3], Adders [1], [7]–[9] and ALU [10]) that focus on optimizing the design parameters. Adders implemented in the previously described works have the major drawbacks of complex carry propagation path and leads to large delay. A technique has been proposed to overcome this drawback by using a binary prefix-based network for carry propagation which leads to low delay.

## II. MATERIALS AND METHODS

This design is mainly based on the concept of carry propagate-generate. Fig. 1 shows the block level implementation of the proposed 3-bit ternary prefix adder. Here  $A(A_2A_1A_0)$ ,  $B(B_2B_1B_0)$  and  $C_{in}$  are ternary inputs and  $SUM(SUM_2SUM_1SUM_0)$ ,  $C_{out}$  are ternary outputs. The intermediate signals which are binary signal and are represented by notation  $X_i^j$ , corresponds to ternary signal  $X_i$ , where  $i$  represents the position of bits and  $j$  represents the logic value i.e., either logic 0 or logic 2 (or  $j \in \{0,1,2\}$ ).



The block level implementation that is shown in the above fig 1, which have six stages in total.

In stage 1, a decoder is given which convert all ternary input to binary logic that is either 0 or 1. And each decoder has one input and three output. For eg. If we are giving  $A_0$  as 1 (ie,  $V_{dd}/2$ ), then the  $X_0^1$  output will be high and all others are low.

$$X_k = \begin{cases} 2, & \text{if } X = k \\ 0, & \text{if } X \neq k \end{cases} \quad (1)$$

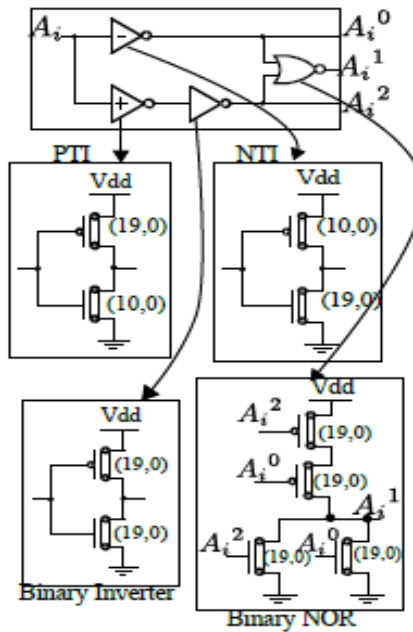


Fig. 2: Ternary Decoder

In stage 2, Here the transformation of binary signals to corresponding intermediate operands ( $HS_2HS_1HS_0$  and  $HC_2HC_1HC_0$ ) occurs. This is achieved by using Half-Adder which in turns consist of a half-sum generator and a half-carry generator.

$$HS_i^2 = A_i^2 \cdot B_i^0 + A_i^1 \cdot B_i^1 + A_i^0 \cdot B_i^2 \quad (2)$$

$$HS_i^1 = A_i^2 \cdot B_i^1 + A_i^1 \cdot B_i^0 + A_i^0 \cdot B_i^1 \quad (3)$$

$$HS_i^0 = A_i^2 \cdot B_i^1 + A_i^1 \cdot B_i^2 + A_i^0 \cdot B_i^0 \quad (4)$$

$$HC_i^1 = A_i^2 \cdot B_i^1 + A_i^2 \cdot B_i^2 + A_i^1 \cdot B_i^2 \quad (5)$$

CNFET based circuit diagram is shown in fig. 3.

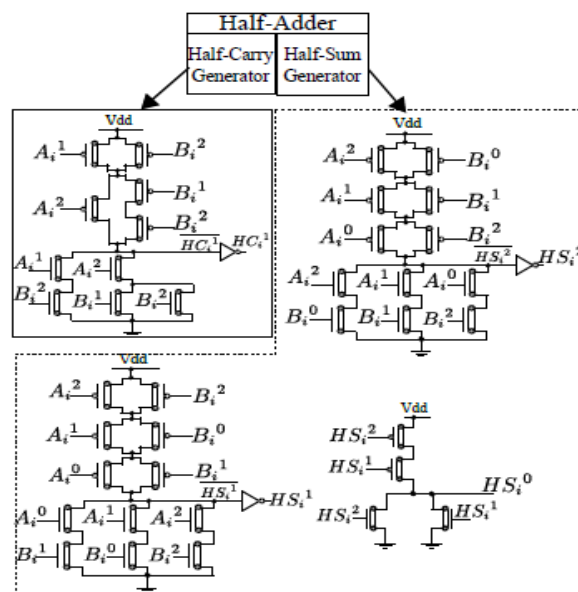


Fig. 3: Half-Adder

In stage 3, this stage contains both simplified half sum generator and simplified half carry generator which generates the half sum ( $THS_i$ ) and half carry ( $THC_i$ ) respectively from the previous output  $HS_i$  and  $HC_{i-1}$ . The logical expression for the sum and carry can be determined as below:

$$THS_i^2 = HS_i^1 \cdot HC_{i-1}^1 + HS_i^2 \cdot \overline{HC_{i-1}^1} \quad (6)$$

$$THS_i^1 = HS_i^1 \cdot \overline{HC_{i-1}^1} + HS_i^0 \cdot HC_{i-1}^1 \quad (7)$$

$$THC_i^1 = HS_i^2 \cdot HC_{i-1}^1 \quad (8)$$

Circuit diagram for the 3<sup>rd</sup> stage is shown in fig. 4

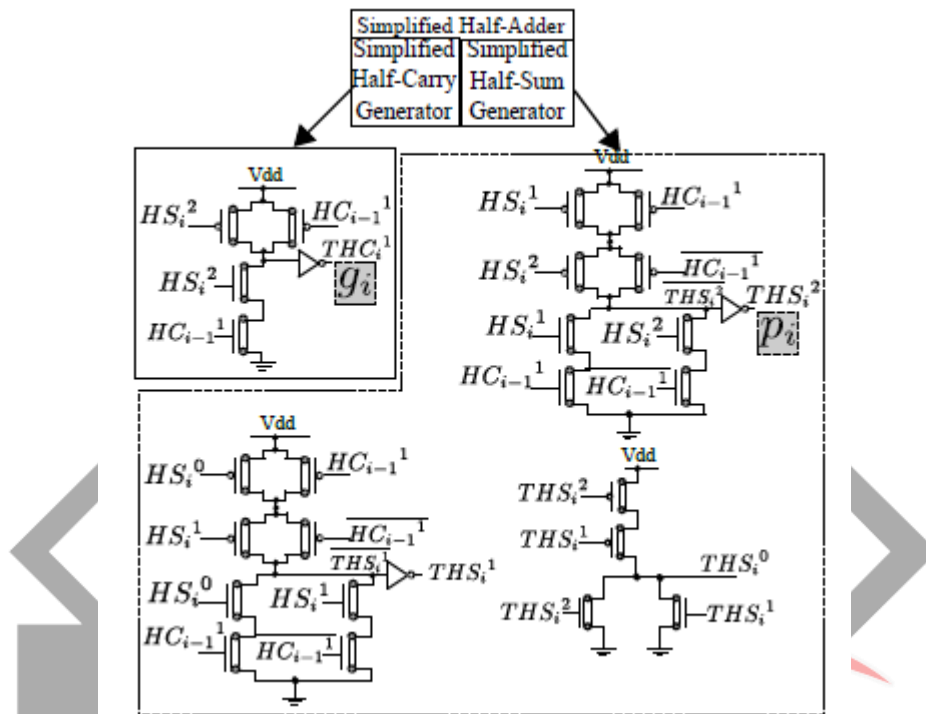


Fig. 4: Simplified Half-Adder

Based on the carry generate and carry propagate condition of an adder, if  $THS_i$  is 2 then the input carry propagates to output. Otherwise carry is the same as half carry  $THC_i$ . Here carry propagate and generate are defined by mathematical equations and is given below.

$$p_i = THS_i^2 = HS_i^1 \cdot HC_{i-1}^1 + HS_i^2 \cdot \overline{HC_{i-1}^1} \quad (9)$$

$$g_i = THC_i^1 = HS_i^2 \cdot HC_{i-1}^1 \quad (10)$$

And then this  $g_i$  and  $p_i$  are taken into the prefix-based carry propagation network for carry computation of ternary input. Prefix-based carry propagation can be defined by equation (11), (12) and (13) respectively. In this work, we have used Kogge-Stone based prefix network (Fig. 5)

$$G_{[i:0]} = TCout_i^1 = g_i + p_i \cdot TCout_{i-1}^1 \quad (11)$$

$$= THC_i^1 + THS_i^2 \cdot TCout_{i-1}^1 \quad (12)$$

$$P_{[i:j]} = p_i \cdot g_j = THS_i^2 \cdot THS_j^2 \quad (13)$$

$$G_{[i:j]} = g_i + p_i \cdot g_j = THC_i^1 + THS_i^2 \cdot THC_j^1 \quad (14)$$

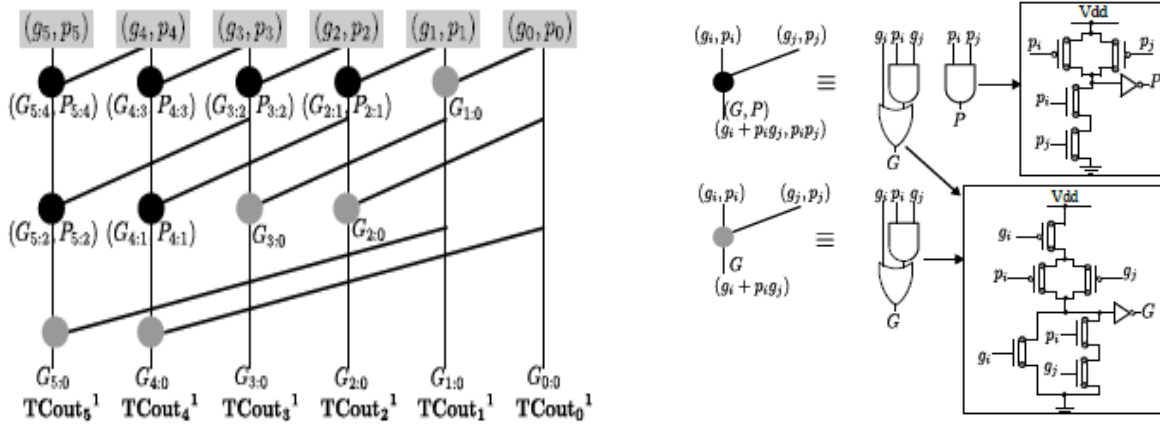


Fig. 5: Kogge-Stone Based Prefix Network

After all the  $TCout_i^1$  (ie, carry) are computed, all binary sum output from stage 4 is fed into stage 6 which consist of only simplified half sum generator for computing  $Sum_i$ . The logical expression for  $Sum_i$  is given below:

$$Sum_i^2 = THS_i^2 \cdot \overline{TCout_i^1} + THS_i^1 \cdot TCout_i^1 \quad (15)$$

$$Sum_i^1 = THS_i^1 \cdot \overline{TCout_i^1} + THS_i^0 \cdot TCout_i^1 \quad (16)$$

Final binary carryout ( $Cout_{N-1}$ ) can be generated by using NOR and NAND gate. The logical expressions for  $Cout_{N-1}^2$  and  $Cout_{N-1}^0$  are given below:

$$\overline{Cout_{N-1}^2} = \overline{HC_{N-1}^1 \cdot TCout_{N-1}^1} \quad (17)$$

$$Cout_{N-1}^0 = \overline{HC_{N-1}^1 + TCout_{N-1}^1} \quad (18)$$

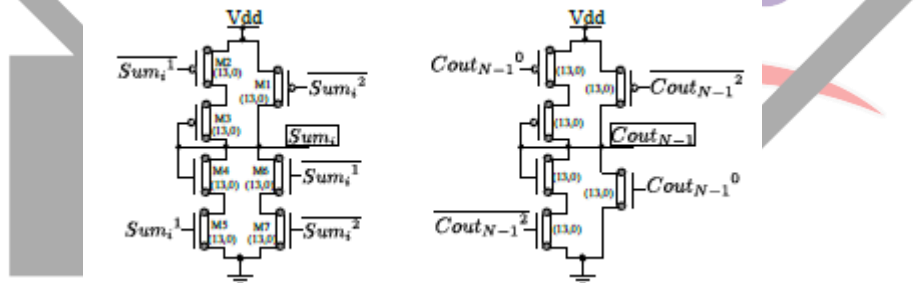


Fig. 7: Ternary Encoder

In the last stage of the proposed adder, i.e. stage 6, which consist of a critical element called encoder and that convert all the intermediate binary signals to ternary signals. One of the major disadvantages of the existing ternary adder design [1], [8] is that they use an encoder which has a low resistance path between VDD and GND to generate logic 1. This increases static current as well as static power consumption. Improved encoders, which uses transistors of the same chirality have been presented in [11]. Fig. 7 shows the improved version of encoders for computing both sum and carry out.

### III. RESULTS AND DISCUSSION

The proposed system is simulated in HSPICE using CNFET model with 32nm channel length and 20nm pitch value at 0.9V power supply and room temperature. Here the ternary logic values 0,1 and 2 correspond to voltages 0, Vdd/2 and Vdd respectively. For binary logic, 0 and 1 correspond to 0 and Vdd respectively. Simulation waveform for Kogge-Stone based prefix adder is shown in Fig. 8

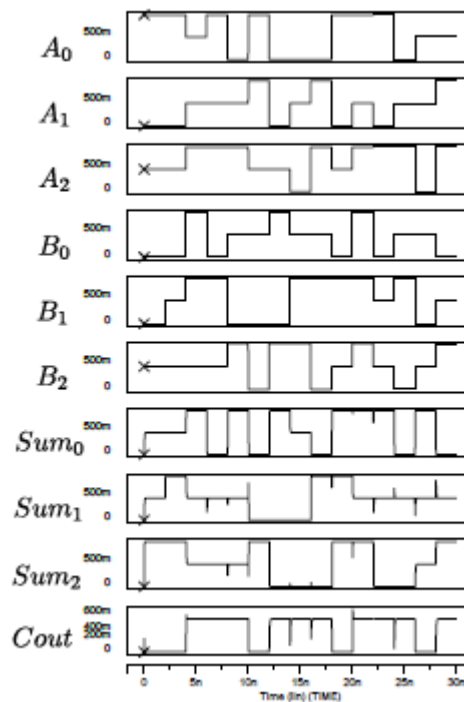


Fig. 8: Waveform for Kogge-Stone Based Prefix Network

Multi-Valued Ternary Adders (MTA), which are implemented using Carry Propagate-Generate concept when compared with previously implemented designs shows a reduction in power consumption and propagation delay by 79% and 69% respectively which are shown in the table given below.

N	Power consumption (uW)
MTA-1	5.69
Proposed Adder	3.214

Table 1: Power Consumption for A 3-Bit Adder

N	Propagation Delay (ps)
MTA-2	64.50
Proposed Adder	17.88

Table 2: Propagation Delay for A 3-Bit Adder

#### IV. CONCLUSION AND FUTURE SCOPE

A 3-bit ternary full adder using carry propagate-generate concept is implemented in this paper and this shows a reduction in delay and power consumption of about 72% and 43% from all other previous works. Here a Kogge Stone based carry prefix network is used for carry computation. All the circuits or blocks have been implemented in HSPICE using CNFET technology

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