DESIGN AND ANALYSIS OF PHASE LOCKED LOOP

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***Abstract*: This paper focuses on the redesign of a PLL system using the 45nm CMOS technology (GPDK045library) in CADENCE Vertuoso Analog Design Environment. The proposed PLL architecture includes following modules: phase and frequency detector(PFD) to compare phase (or frequency) of input reference and phase(or frequency) of feedback signal and generate the difference or an error signal, charge pump and loop filter is to convert the digital UP and DOWN signals into analog control voltage, voltage controlled oscillator is to produce the clock output which is the multiplication of the input reference frequency and multiplication factor(N) and frequency divider is to equal the output frequency with input frequency. All modules are integrated in order produce the 1GHz output frequency from 4MHz input frequency at 1.8V DC supply and have lock time 40µs. Output clock have period jitter 44.87ps.**

***Keywords:* phase locked loop, charge pump, phase and frequency detector, voltage controlled oscillator and lock time.**

I. INTRODUCTION

Phase locked loop (PLL) is an important block of the modern electronic system as well as communication system. The most widely used application of the PLL is for clock recovery and clock generation in microprocessor, communication and networking system. Recently many of the researches carried out on the PLL and still research is going on to understand a higher lock range PLL with lesser lock time. PLL as become one of the major block in the electronics technology, Since the development in the area of integrated circuits. PLL architecture contains both digital and analog signal circuits, so that PLL acts like mixed signal circuit which includes design challenges at high frequency.

The standard Phase locked loop having 5 main blocks, they are phase and frequency detector (PFD), charge pump (CP), Loop filter (LPF), Voltage controlled oscillator and Frequency divider. There are three types of existing PLL architectures are used to design PLL which are, Analog PLL (APLL), Digital PLL(DPLL) and All Digital PLL(ADPLL). The proposed PLL block diagram showing in Fig.1, the PFD compares feedback signal (VCO output) with reference input signal, two output signals are produced i.e. up and down pulses which depends on phase and frequency difference between the reference and feedback signals. UP and DOWN signals are applied to the Charge pump which converts these digital signals into analog current which flow into or out of loop filter that is charging or discharging the capacitor and hence increase or decrease the VCO output frequency and then feedback to the PFD through frequency divider which divides the VCO output frequency by 256 and equals to the reference frequency and this process is continuous till the phase locks.

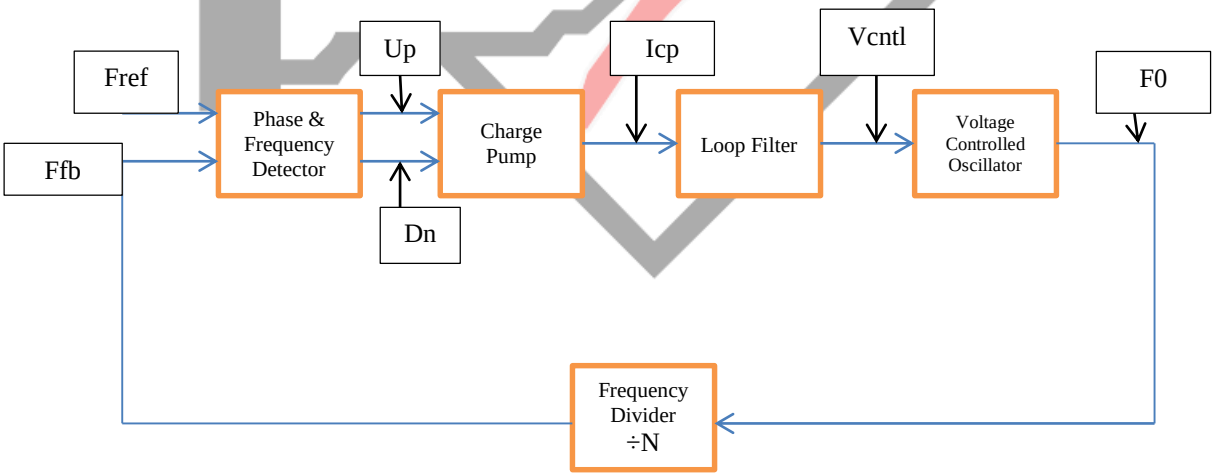

Fig.1: PLL block diagram.

II. PRIOR WORK

Presently most of the communication and electronic systems include different types of processors which operate at high frequency clock. Usually the clocks are supplied to these processors came from Local oscillator which are low frequency clocks (Typically 10 or 100MHz). If we want high frequency clocks, we have to use PLL which is simply multiplies the low frequency reference clock with multiplication factor and produces the high frequency clock. Difficult to set the delay of each stage in digitally controlled oscillator and DCO have more complex design. The traditional architecture generates the 800MHz output from 100MHz input so here they use one more oscillator to produce the reference frequency hence it consumes more area. To avoid all these

problems, there is architecture that utilizes lowest input frequency and VCO instead of DCO and generates 1GHz output from 4MHz input.

III. Architecture and Circuit Design

The PLL finds wide application in microcontroller to control the clock signals frequency. This can give the opportunity for microcontroller to run at frequency of the clock is faster than the oscillator itself. This paper proposes design strategy for charge pump based PLL, which is analog PLL. The main objective of this project is to Design of Gigahertz Phase Locked Loop in 45nm CMOS technology. The proposed PLL architecture consists of five modules which are phase and frequency detector (PFD), charge pump (CP), loop filter (LPF), voltage controlled oscillator (VCO) and frequency divider (÷256).

A. Phase and Frequency Detector

It compares input reference signal and feedback signal produces the error or difference signal as shown in Fig.2. This output is linearly proportional to the phase difference($\Delta\emptyset$) between its two inputs.

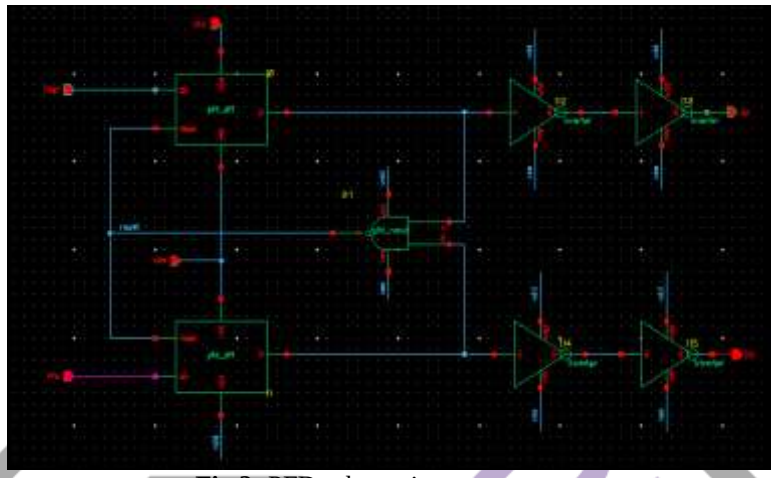

Fig.2: PFD schematic structure.

Fig.2 shows the schematic structure of PFD, it consists of two D-flip flops and AND gate. For top D-flip flop, reference input signal (F_{ref}) is applied to clock terminal, and VDD is connected to data terminal. For bottom D-flip flop, feedback signal (Ffbk) is applied to the clock terminal and data terminal is connected to VDD. The reset signal is given to the reset terminal of both the D-flip flops. initially up = dn =0, when Fref goes high as a result up signal also goes high and eventually followed by rising edge of Ffbk, dn signal rises and the NAND gate resets both the signal. Alternatively say up and dn signals are rises for small time. But the difference between their average values represent the frequency or phase difference of the input signals correctly. From observing the Fig.2, Buffer is placed at the each output side to drive the next stage.

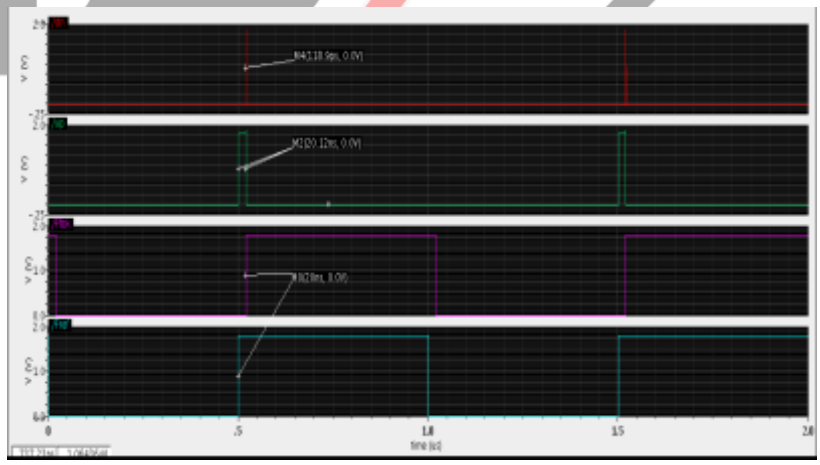

Fig.3 (a): PFD output when reference signal(Fref) leads feedback signal(Ffbk).

Fig 3 (a)and (b) shows the output waveforms of the PFD for two conditions i) phase of input reference signal (Fref) leads phase of feedback signal (Ffbk) and ii) phase of input reference signal (Fref) lags phase of feedback signal (Ffbk).

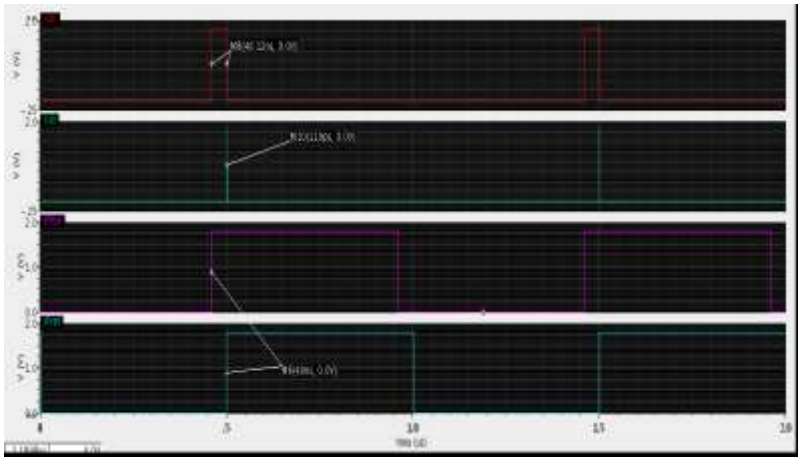

Fig.3(b): PFD output when reference signal(Fref) lags Ffbk.

B. Charge Pump and Loop Filter

Charge pump circuit is used to combine the both PFD outputs (UP and DOWN) and gives the single output I_P, which is utilized to charge or discharge the capacitor in loop filter.

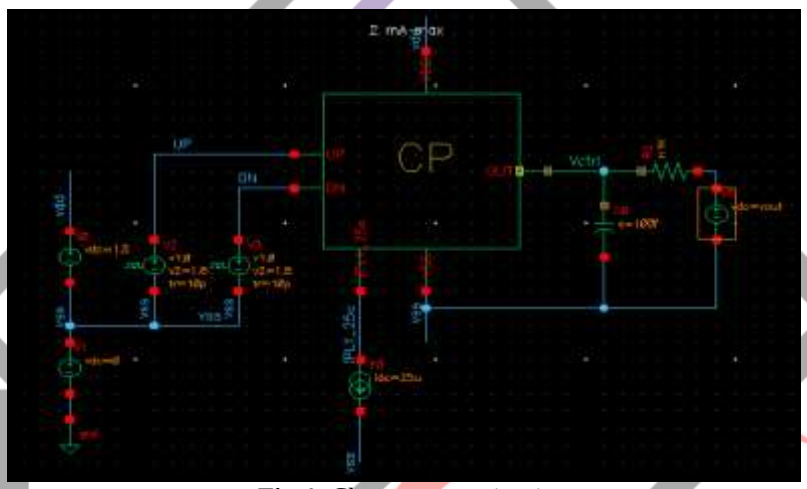

Fig.4: Charge pump circuit

When UP signal is high, source current enables i.e. source current will flow into the loop filter, charge the capacitor as a result increase the control voltage and hence increase the VCO output frequency. when DOWN signal is high sink current enables i.e. sink current flows out of the loop filter, discharge the capacitor hence decrease the control voltage as a result decrease the VCO output frequency and when both UP and DOWN signals are low, no current will flow into the loop filter hence constant voltage and constant VCO output as shown in Fig.5.

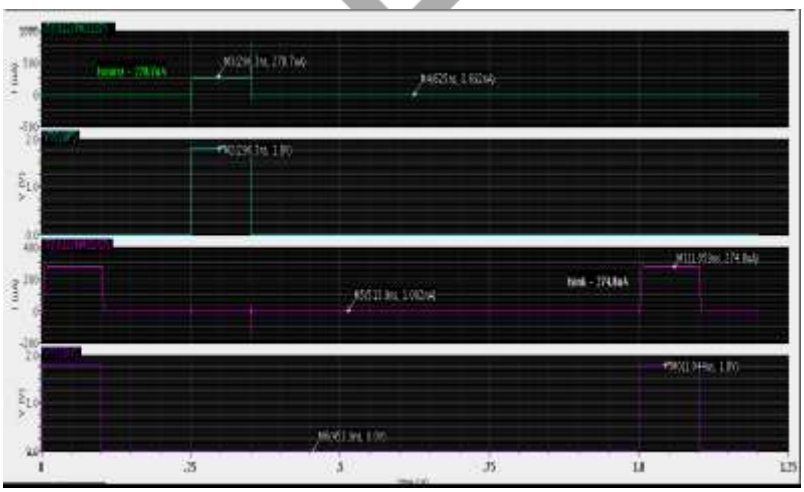

Fig.5: Charge pump output waveform.

C. Voltage Controlled Oscillator

Voltage Controlled Oscillator is most important block in PLL as shown in Fig.6. VCO generates clock signal and its output frequency can be varied by changing the input control voltage.

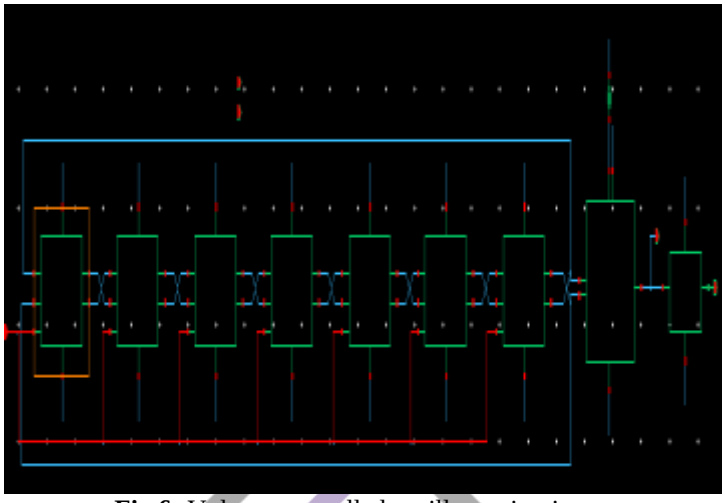

Fig.6: Voltage controlled oscillator circuit.

In today's technology most widely used CMOS oscillator is ring oscillator, single ended ring oscillators involves difficulty in obtaining the time delay(T_d) due to nonlinearities and parasitics of the circuit. To avoid the conflict between the oscillation speed and multiphase output, here i taken the differential ring oscillator it consists of 7 gain stages in a loop and there is an inversion between each stages as shown in fig.6. this circuit have more advantages, which produces the 50% duty cycle at the output, better immunity to common mode noise and it is not restricted to have odd number of stages so that it gives more flexibility in changing the oscillation frequency because ring oscillators also have high frequency tuning range. The oscillation frequency is given by,

$$F_{out} = \frac{1}{2NTd} \quad (1)$$

Where,

N - Number of stages.

T_d - delay of each cell,

$$T_d = \frac{1}{2NFout}$$

Given, Fout = 1GHz and N=7

$$\therefore \quad T_d = \frac{1}{2x7x1x10^9} = 71.42ps$$

Here, there is 1.00GHZ output frequency at Vctrl=1.187 as shown in Fig.7. If we vary the control voltage (Vctrl), output frequency also varies. Fig.8 shows the transfer characteristics of vco which is the plot of output frequency versus input control voltage (Vctrl), using this plot we can say- this circuit should be linear and also find the vco gain i.e.$\frac{\Delta Y}{\Delta X}$ = 0.705G. For minimum control voltage Vctrl=0.7V, vco output is 110.4MHz and For maximum control voltage Vctrl=1.8V, vco output is 1.88GHz, therefore vco output frequency range is 110.4MHz to 1.88GHz as shown in Fig.8.

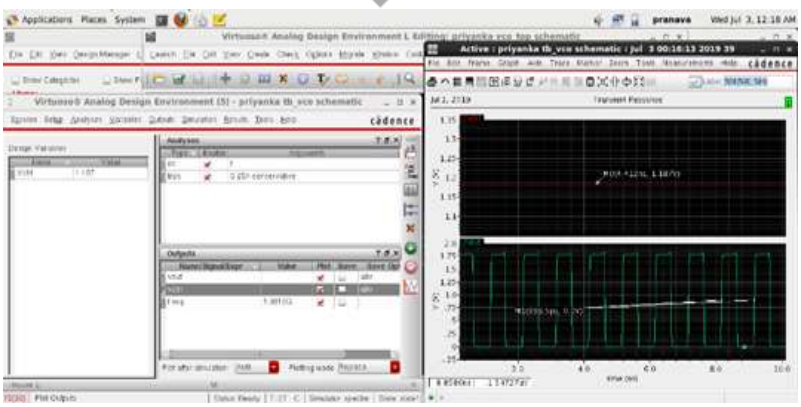

Fig.7: VCO output waveform.

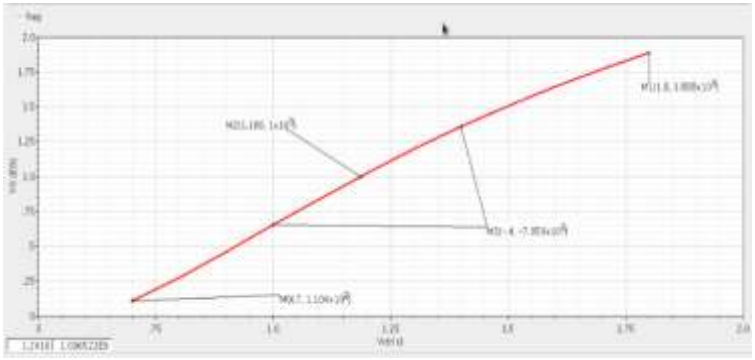

Fig.8: Transfer characteristics of VCO.

C. Frequency Divider

Function of the frequency divider is to scales down the VCO output frequency by a factor N and equals to input reference frequency. This circuit as shown in Fig.9 which is placed in between the VCO and PFD circuit, that is in feedback path.

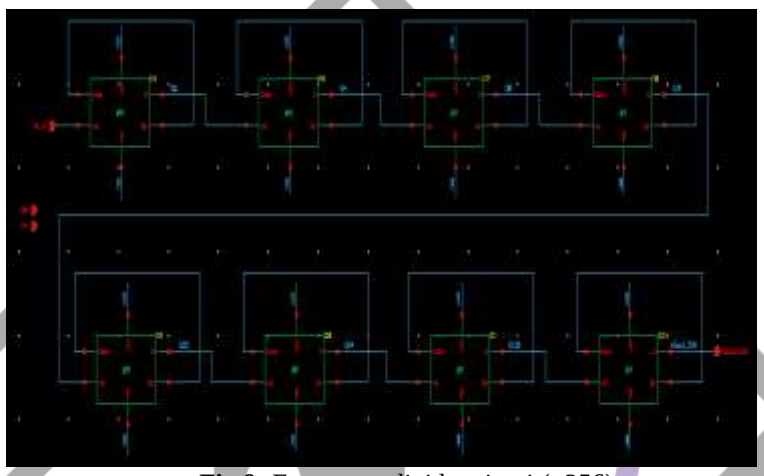

Fig.9: Frequency divider circuit(÷256).

When 1GHZ VCO output is passing through the ÷256 network, there is 4MHz output as shown in fig.10.

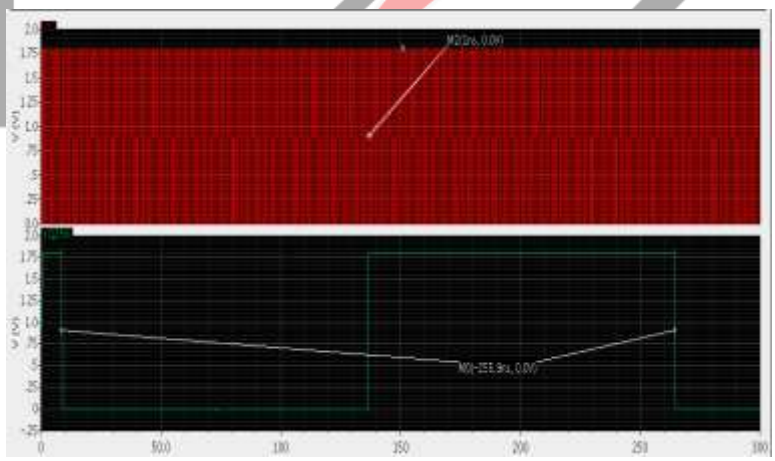

Fig.10: Frequency divider output waveform.

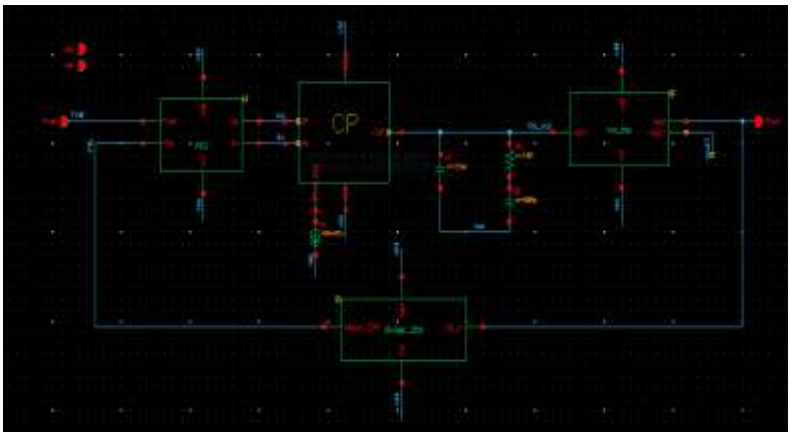

Fig.11: Proposed PLL Architecture.

All above explained circuits are integrated in order to generate the 1GHz output from 4MHz input as shown in Fig.11. The PLL is in locked condition at 1GHz and within 40µs time cycle.

IV. RESULT

The integrated Phase Locked Loop circuit is designed and simulated. The control voltage variation as shown in the Fig.12, The output of the loop filter circuit means the control voltage (Vctrl) maintain a constant value when the reference input signal (Fref) and feedback signal (Fout) are in lock. From the Fig.12, it's clear that the control voltage maintains the constant value of 0.885V within 40µs time cycle.

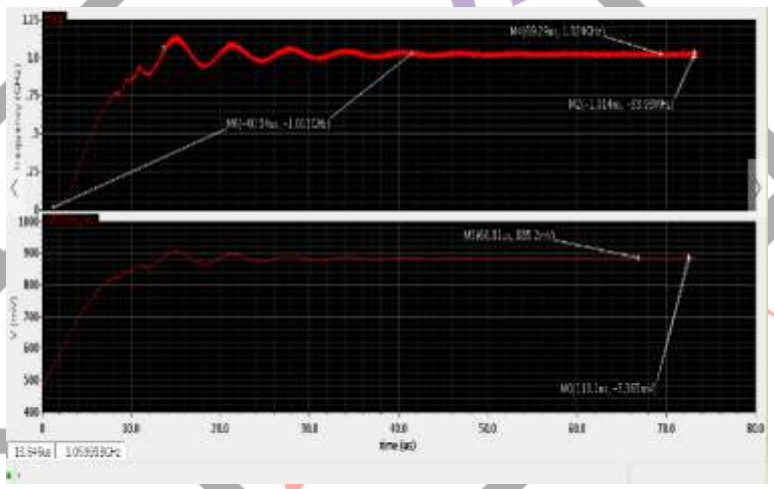

Fig.12. Output frequency and control voltage(Vctrl) versus time.

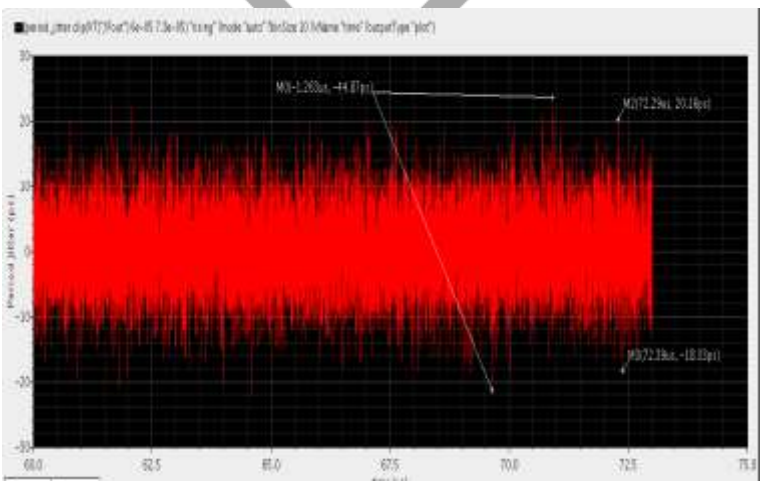

Fig.13. Period jitter of PLL output.

The PLL is locked at 1GHz frequency as shown in Fig.12. Time elapsed between PLL power on and the time at which 1GHz occur is called lock time. The lock time is 40µs. PLL output have jitter = 44.87ps as shown in Fig.13.

TABLE I
Performance summary and Comparison of traditional PLL with proposed PLL.

References	[1]	[3]	Conventional work.	Proposed work
Technology	180nm	130nm	90nm	45nm
Supply voltage	1.2V	1V	1V	1.8V
Frequency range	155.4MHz	100-400MHz	100MHz-1GHZ	4MHz
Locked time	X	X	2.82ns	40µs
period jitter	X	5.81ps	4.223ps	44.87ps

V. CONCLUSION

The main objective of this project is to redesign the PLL at 45nm CMOS technology and produces 1GHz output frequency from 4MHz input reference frequency at supply voltage of 1.8V. After this PLL continuous to produce the output even though in lock mode, the PLL output is constant. This design Output frequency is the multiplication of input reference frequency(4MHz) and integer factor(256) and also find the lock time =40µs and period jitter = 44.87ps. This PLL architecture can be used as frequency multiplier.

The proposed architecture is utilized for various analog applications and clock system. To further reduce the lock time and design the programmable divider for many areas of electronics and RF applications and also to design the digitally controlled oscillator for different digital applications. In future, it can be taken as good reference for designing the PLL using different approaches.

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