Delay variation model for conventional Wallace tree multiplier and 4:2 compressor

[1]B.Aswand, [2]S.Kayalvizhi, [3]K.Sangeetha

PG Scholars
Electronics communication engineering,
Government college of Technology, Coimbatore.

***Abstract*: Multipliers play a vital role in in high performance systems, So the performance of multiplier is improved by Wallace tree multiplier. The Wallace Tree Multiplier is considered as faster than conventional wallace tree multiplier. At the same time Low power circuit designs have been an important issue in VLSI designs areas. This can be achieved by compressor. Respective speed of the multiplier is improved by higher order compressor. This paper proposes the comparison of 4 bit, 8 bit conventional Wallace tree multiplier with 4:2 compressor. The coding is done on Verilog HDL and synthesis is done by using Xilinx ISE 14.7.Further analysis and layout is done by using cadence encounter tool.**
***Index Terms*—Component, formatting, style, styling, insert.**

***Keywords*: cadence encounter tool, Xilinx ISE 14.7, 4:2 compressor**

I. INTRODUCTION

A multiplier is one of the key hardware blocks in most digital signal processing (DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications. Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design. A system performances generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issues. However, area and speed are usually conflicting constraints so that improving seed results mostly in large areas. Fast multipliers are essential parts of digital signal processing systems. The speed of multiply operation is great importance in digital signal processing as well as in the general purpose processors today, especially since the media processing took off. In the past multiplication was generally implemented via a sequence of addition, Subtraction and shift operations. Multiplication can be considered as a series of repeated additions. The number to be added is the multiplicand, the number of times that is added is the multiplier and the result is product. Each step of addition generates a partial product. By using different algorithm the number of partial product can be reduced which result in reduced area and delay.

The multiplication operation involves generation of partial products and their accumulation. The speed of multiplication can be increased by reducing the number of partial products and/or accelerating the accumulation of partial products. Among the many methods of implementing high speed parallel multipliers, the basic approach for this is namely Wallace Tree compressors.

The conventional Wallace tree multiplier is based on carry save adder. Here the speed of the multiplier is improved by introducing compressors instead of the carry save adder. 4-2 compressor are used with Wallace tree multiplier. Higher order compressors have better performance compared with 3-2 compressor. So the speed of the multiplier can be improved by introducing the higher order compressors.

II.FLOW GRAPH:

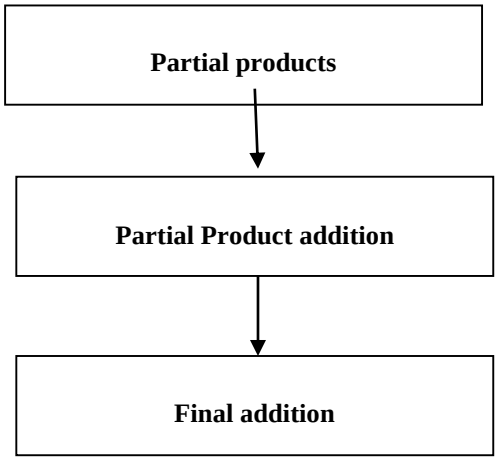


Fig.1conventional Wallace tree multiplier

A. Partial products:

This partial product multiplication is works exactly like long hand multiplication. Binary numbers are product and results of simple AND gate. All the products and done simultaneous sly. Requires a lot of hardware (i.e n^2 AND gates).

B. Partial products addition:

To add up columns, add up three rows at a time full adder and half adder is used three bits are added by full adder, two bits are added by half adder. The resulting set of two rows has a row for the sum and row for the carry-out, left alone the odd rows, further repeat the process. This time, there are two sets of three rows result is two sets of two rows. This stage take lot of hardware as well, repeat the process this time there's only one set of three rows, plus an extra row to carry down. Each step takes as long as a full adder because this is the slowest part. All adders are done in parallel, repeat the process for one last time. Remaining three rows become two rows.

C. Final addition:

Final result is calculated by adding the final two rows. The savings from already having 5bit offsets the delay from doing partial product addition. Result is that Wallace tree multiplication takes about the same amount of time as a 2N bit ripple carry adder.

D. Four bit conventional multiplier:

Two 4bit multiplier and multiplicand gives 8 bit final product addition.dot diagram for 4bit conventional multiplier is shown below.

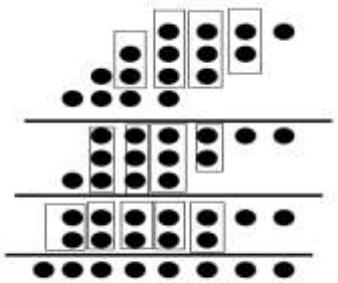


Fig 2. 4 bit Conventional Wallace tree multiplier dot diagram

E. 8 bit conventional multiplier:

Two 8bit multiplier and multiplicand gives 16 bit final product addition.dot diagram for 8bit conventional multiplier is shown below.

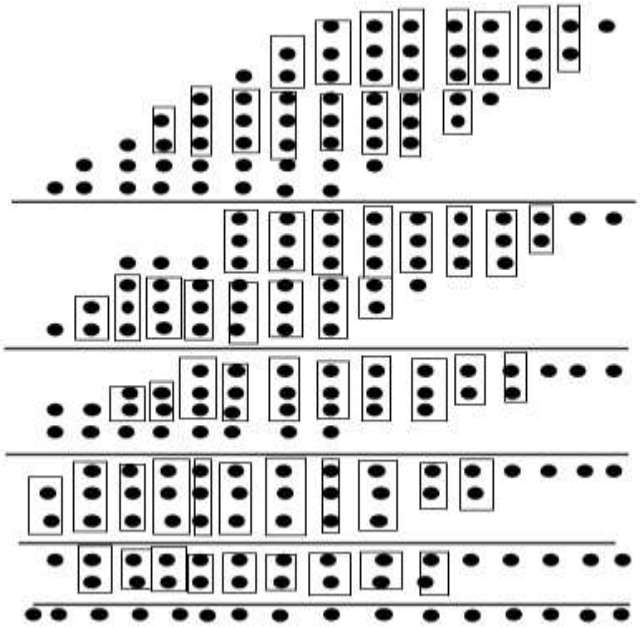


Fig3. 8bit Wallace tree multiplier dot diagram

III.WALLACE TREE MULTIPLIER USING 4:2 COMPRESSORS:

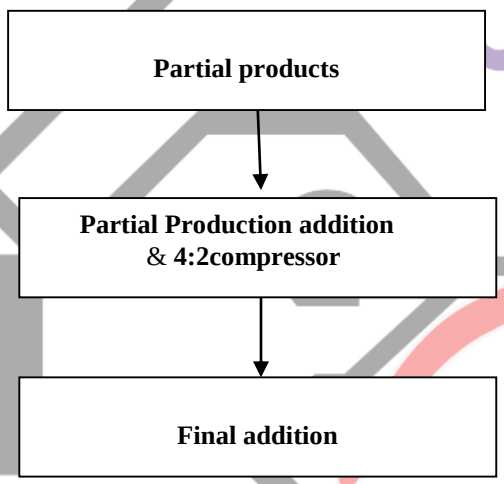


Fig.4 conventional Wallace tree multiplier using 4:2 compressor

Partial products and partial products addition are done as like conventional Wallace tree multiplier only one thing is varied that 4:2 compressor. This can be understood by following block diagram.

A. 4:2 COMPRESSOR:

A compressor is a device which is mostly used in multipliers to reduce the operands while adding terms of partial products. A typical M-N compressor takes M equally weighted input bits and produces N-bit binary number. The simplest and the most widely used compressor is the 3-2 compressor which is also known as a full adder. It has Three inputs to be summed up and provides two outputs. Similarly, a 4-2 compressor can also be built from two Cascaded 3-2 compressor circuits. The conventional implementation of a 4-2 compressor is composed of two serially connected full adders.

One of the major speed enhancement techniques used in modern digital circuits is the ability to add numbers with minimal carry propagation. The basic idea is that three numbers can be reduced to 2, in a 3:2 compressor, by doing the addition while keeping the carries and the sum separate. This means that all of the columns can be added in parallel without relying on the result of the previous column, creating a two output "adder" with a time delay that is independent of the size of its inputs. The sum and carry can be recombined in a normal addition to form the correct result. This process may seem more complicated and pointless, but the power of this technique is that any amount, number of additions can beaded together in this manner. It is only the final recombination of the final carry and sum that requires a carry propagating addition. 3:2 compressor is also known as full adder. It adds three one

bit binary numbers, a sum and a carry. The full adder is usually a component in a cascade of adders. The carry input for the full adder circuit is from the carry output from the cascade circuit. Carry output from full adder is fed to another full adder.

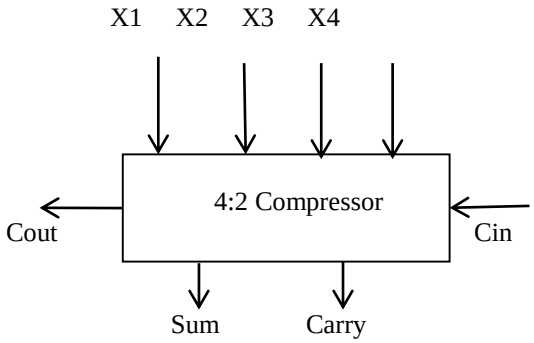


Fig.5 4:2 Compressor

The characteristics of the 4:2 compressors are:

To avoid carry propagation, the value of Cout depends only on A, B, C and D. It is independent of Cin. The Cout signal forms the input to the Cin of a 4:2 of the next column. The common implementation of a 4-2 compressor is accomplished by utilizing two full-adder (FA).

To add binary numbers cells.4:2 compressor is composed of two serially connected full adders. With minimal carry propagation we use compressor adder instead of other adder. Compressor is a digital modern circuit which is used for high speed with minimum gates requires designing technique. This compressor becomes the essential tool for fast multiplication adding technique on fast processor and lesser area.

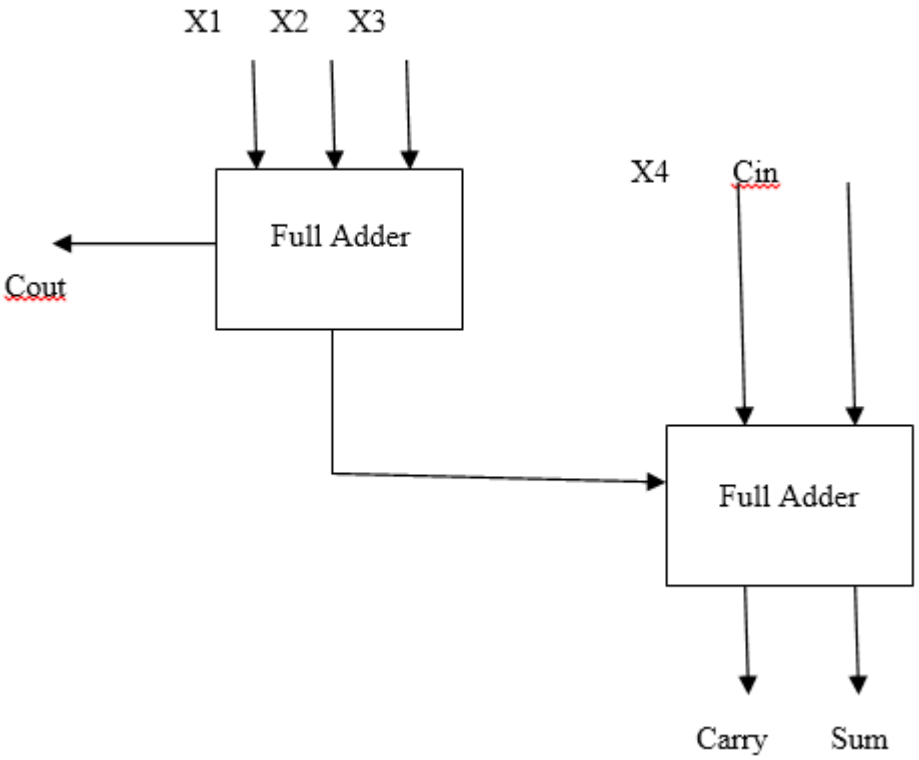


Fig 6.4:2 compressor by 2 full adder

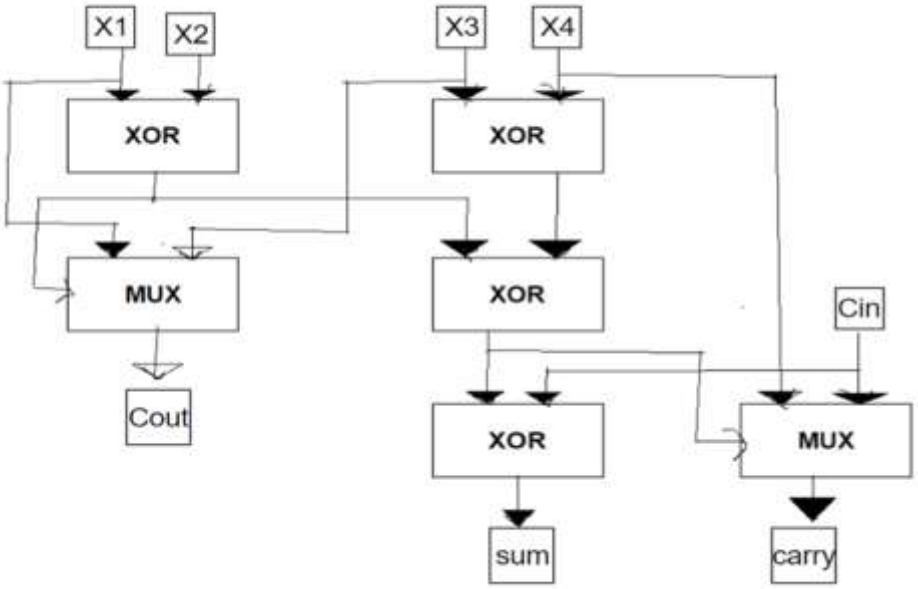
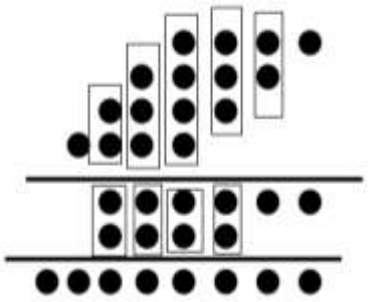


Fig 7. 4:2 compressor by xor module

Sum = x1 x2 x3 x4 c in
C out = (x1 x2) x3+ (x1 x2) ` x1
Carry = (x1 x2 x3 x4) c in+(x1 x2 x3 x4) `x4

B. 4bit Wallace tree multiplier using 4:2 compressor:

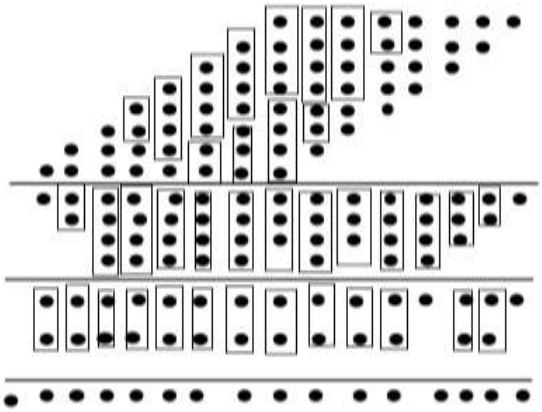
Dot diagram for 4bit Wallace tree multiplier using 4:2 compressor is shown below. by comparing with 4bit conventional Wallace tree multiplier 3 stage is reduce in to 2 stage. Operation need to be perform also reduced 4bit Wallace tree multiplier:



C. 8bit Wallace tree multiplier using 4:2 compressor :

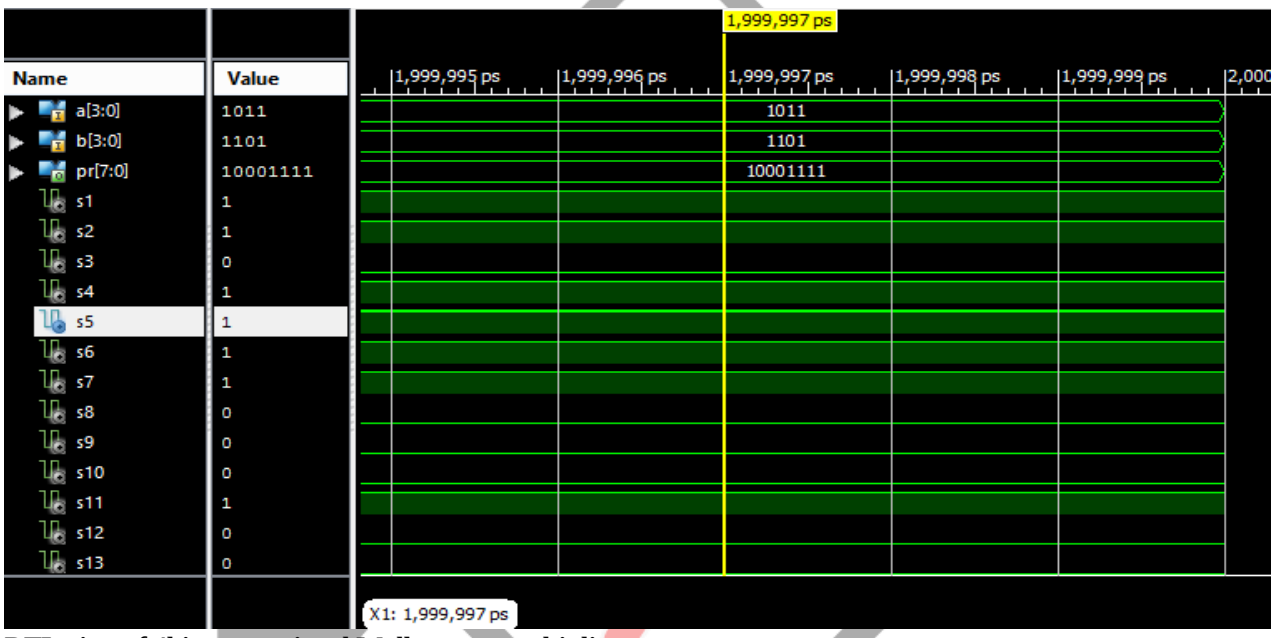
Dot diagram for 8bit Wallace tree multiplier using 4:2 compressor is shown below. by comparing with 8bit conventional Wallace tree multiplier 5 stage is reduce in to 3 stage. Operation need to be perform also reduced 4:2 compressors are capable of adding 4 bits and one carry, in turn producing a 3 bit output. The 4-2 compressor has 4 inputs X1, X2, X3 and X4 and 2 outputs Sum and Carry along with a Carry-in (Cin) and a Carry-out (Cout). The input Cin is the output from the previous lower significant compressor.

The Cout is the output to the compressor in the next significant stage. The critical path is smaller in comparison with an equivalent circuit to add 5 bits using full adders. However, like in the case of 3-2 compressor, the fact that both the output and its complement are available at every stage is neglected. Thus replacing some XOR blocks with multiplexer's results in a significant improvement in delay as shown in Fig.4. Also the MUX block at the SUM output gets the select bit before the inputs arrive and this minimizes the delay to a considerable extent.

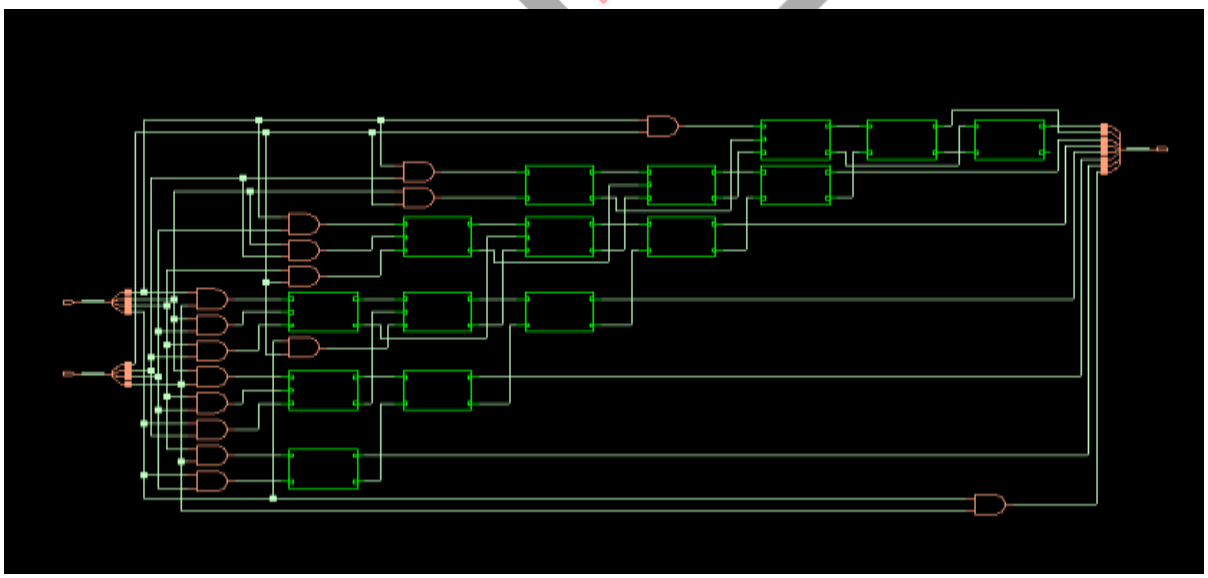


IV.SIMULATION RESULTS

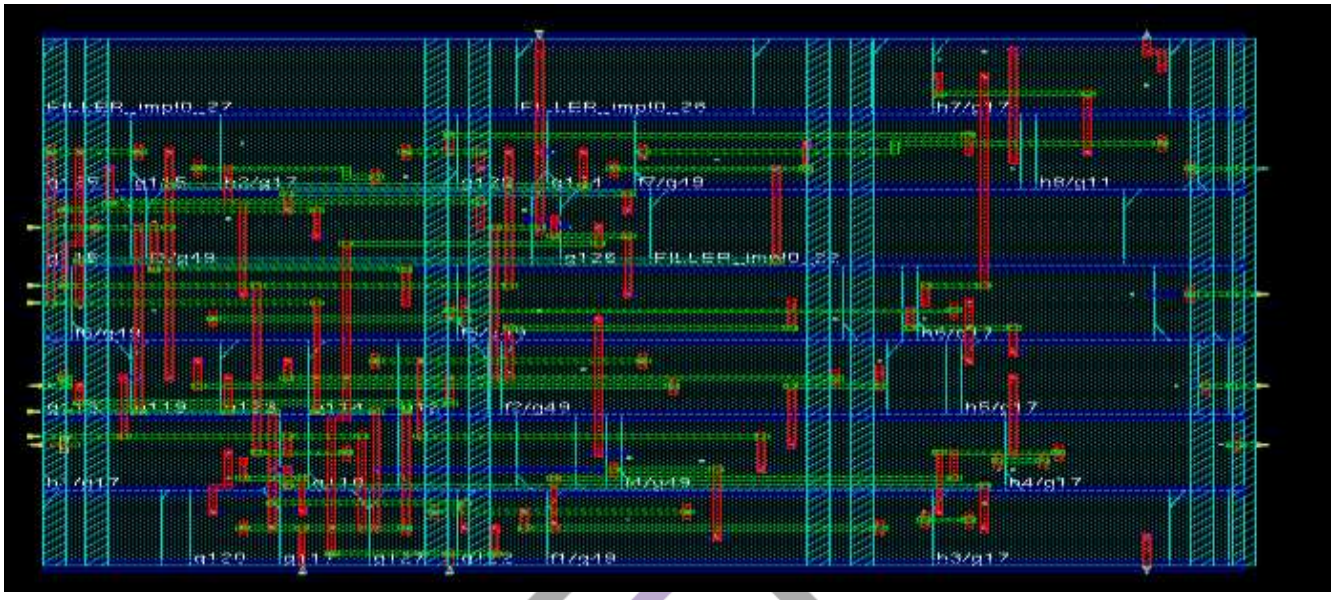
OUTPUT FOR 4 BIT WALLACE TREE MULTIPLIER :



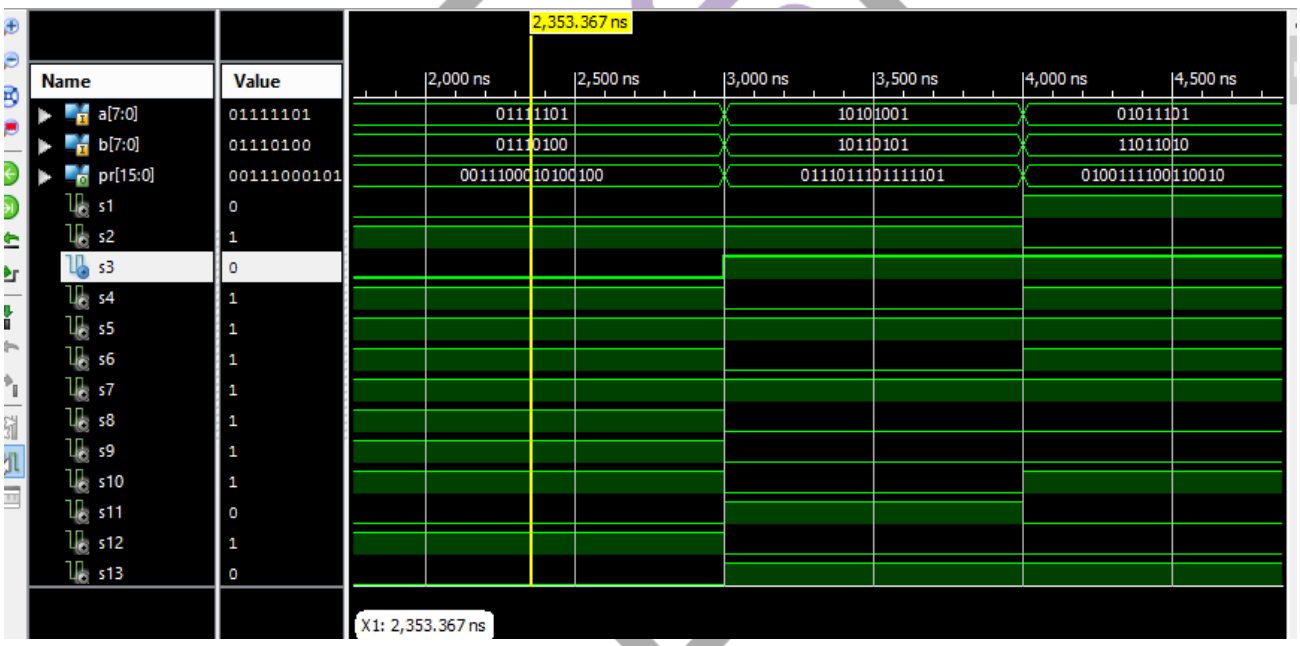
RTL view of 4bit conventional Wallace tree multiplier:



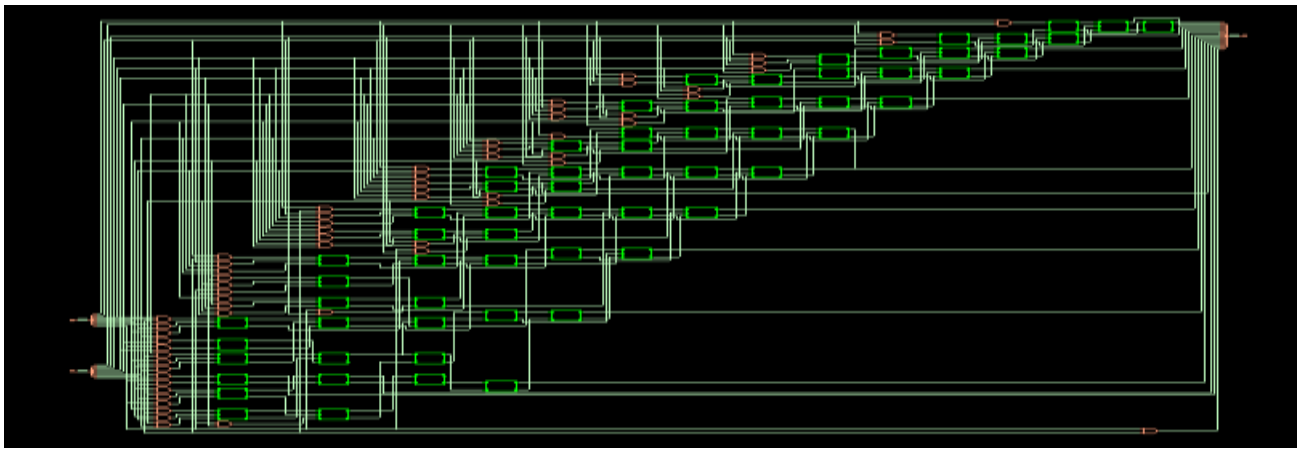
Layout for 4 bit conventional Wallace tree multiplier:



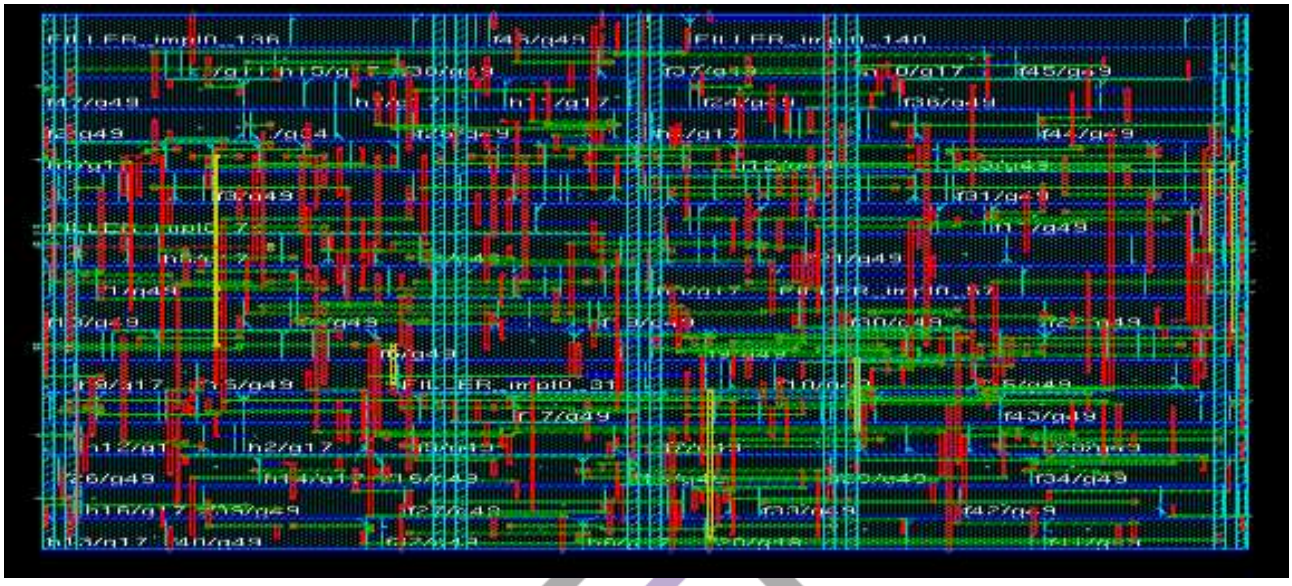
B.8 bit conventional Wallace tree multiplier:



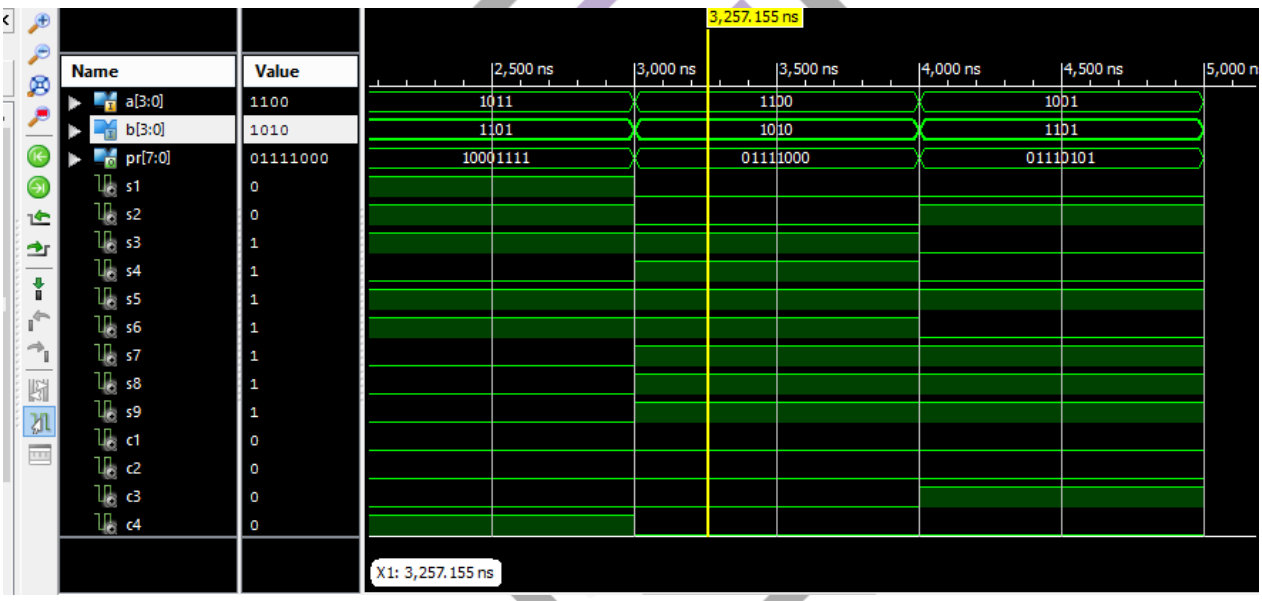
RTL view of 8bit conventional Wallace tree multiplier:



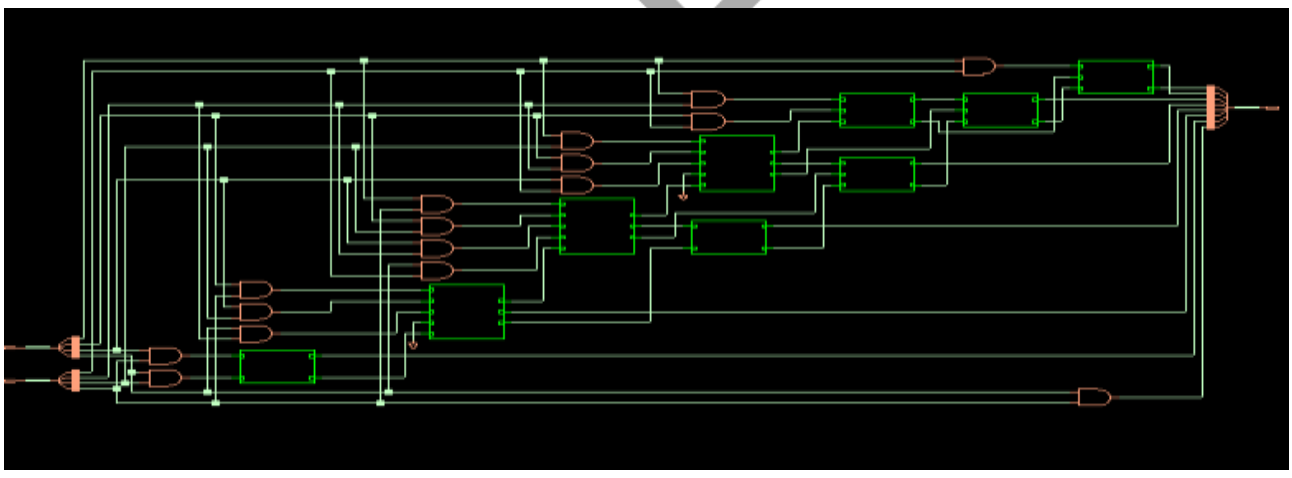
Layout for 8bit conventional Wallace tree multiplier:



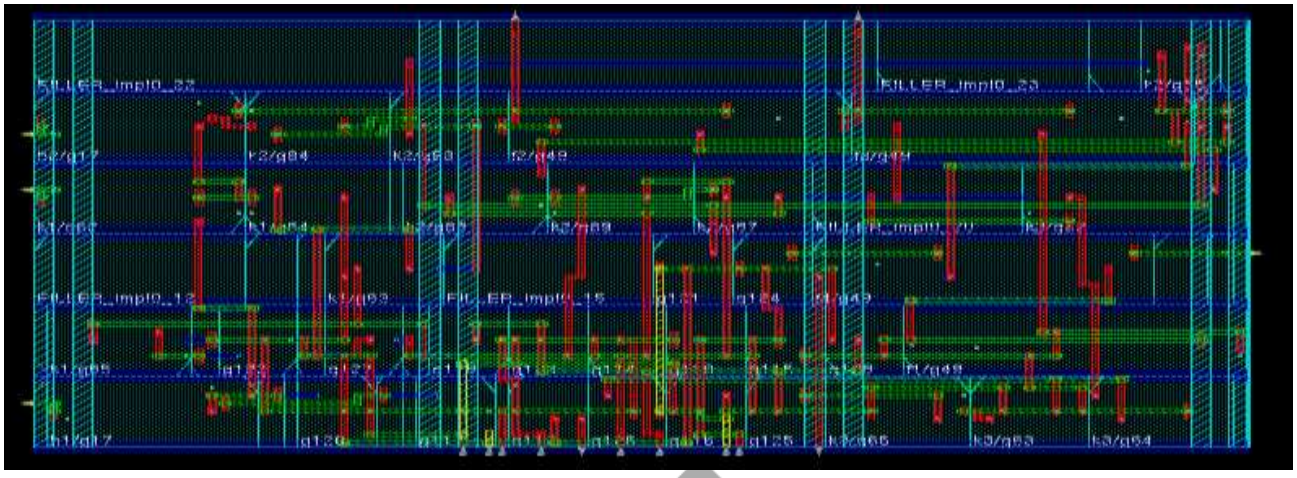
C.4BIT WALLACE TREE MULTIPLIER USING 4:2 COMPRESSOR:



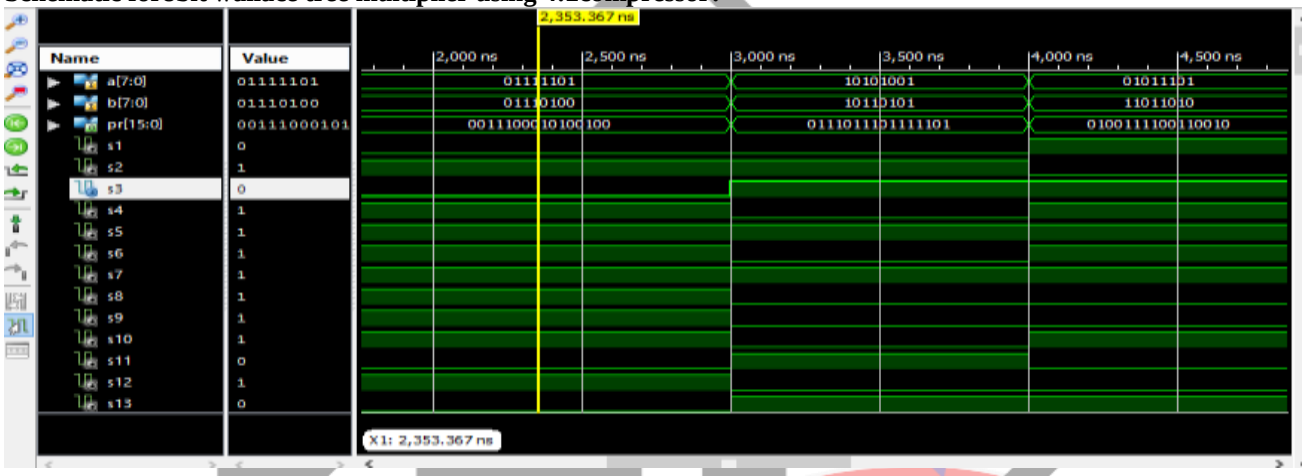
RTL view for 4 bit Wallace tree multiplier using 4:2compressor:



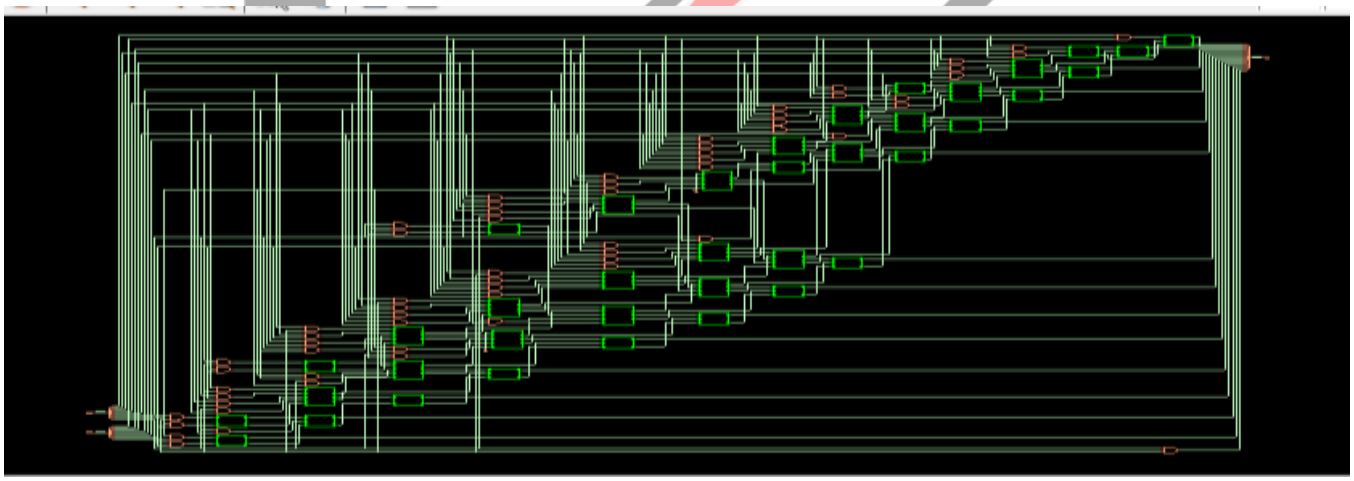
Layout for 4 bit Wallace tree multiplier using 4:2compressor:



Schematic for8bit wallace tree multiplier using 4:2compressor:



RTL view for 8 bit wallace tree multiplier using 4:2compressor:



Layout for 8 bit wallace tree multiplier using 4:2compressor:

Table:1.1 (Time, power, Area Analysis)

		TIMING(ps)	POWER(nW)	AREA(nm)
4 BIT	4 BIT WALLACE TREE MULTIPLIER	389.10	9521.46	303.52
	4 BIT WALLACE TREE MULTIPLIER USING 4:2 COMPRESSOR	22.70	6390.91	292.92
	% OF INCREASE/DECREASE	42.77% (fast)	32.9% (decreased)	3.5% (decreased)
8 BIT	8 BIT WALLACE TREE MULTIPLIER	371.40	63064.66	1406.32
	8 BIT WALLACE TREE MULTIPLIER USING 4:2 COMPRESSOR	221.80	52391.40	1147.19
	% OF INCREASE/DECREASE	+ 40.28% (fast)	17.08% (decreased)	17.4% (decreased)

V. CONCLUSION:

Wallace tree multiplier using 4:2 compressor is the best technique for high speed multiplication but its hard to implement. For higher order multiplication, higher order compressors can be used to compress the bits. Instead of 4:2 compressor using 7:2 compressor we can reduce the power consumption, area and delay.

REFERENCES:

[1] P.APARNA AND N. THOMAS (2012), DESIGN AND IMPLEMENTATION OF A HIGH PERFORMANCE MULTIPLIER USING HDL, COMPUTING, COMMUNICATION AND APPLICATIONS (ICCCA), 2012 INTERNATIONAL CONFERENCE ON. IEEE, PP. 1–5

[2] M. BANSAL, S. NAKHATE, AND A. SOMKUWAR (2011), HIGH PERFORMANCE PIPELINED SIGNED 64X64- BIT MULTIPLIER USING RADIX-32 MODIFIED BOOTH ALGORITHM AND WALLACE STRUCTURE, COMPUTATIONAL INTELLIGENCE AND COMMUNICATION NETWORKS (CICN), 2011 INTERNATIONAL CONFERENCE ON. IEEE, PP. 411– 415.

[3]. WALLACE TREE MULTIPLIER DESIGNS: A PERFORMANCE COMPARISON REVIEW, HIMANSHU BANSAL, K. G. SHARMA, TRIPTI SHARMA, INNOVATIVE SYSTEMS DESIGN AND ENGINEERING ISSN 2222-1727 (PAPER) ISSN 2222-2871 (ONLINE) VOL.5, NO.5, 2014.

[4]. MODIFIED WALLACE TREE MULTIPLIER USING EFFICIENT SQUARE ROOT CARRY SELECT ADDER, PARADHASARADHI, D. PRASHANTHI, M. VIVEK, N. GREEN COMPUTING COMMUNICATION AND ELECTRICAL ENGINEERING (ICGCCEE), 2014 INTERNATIONAL CONFERENCE.

[5] KULVIR SINGH, DILIP KUMAR "MODIFIED BOOTH MULTIPLIER WITH CARRYING SELECT ADDER USING 3-STAGE PIPELINING TECHNIQUE" INTERNATIONAL JOURNAL OF COMPUTER APPLICATIONS (0975 – 8887) VOLUME 44– NO14, APRIL 2012.

[6].D. DAS AND H. RAHAMAN (2010), A NOVEL SIGNED ARRAY MULTIPLIER, ADVANCES IN COMPUTER ENGINEERING (ACE), 2010 INTERNATIONAL CONFERENCE ON. IEEE, PP. 19–2.