# PV INVERTER APPLICATIONS WITH ZERO VOLTAGE TECHNIQUE

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*Abstract*: Soft-switching is inherent owing to the proposed secondary modulation and is maintained during wide variation in voltage and power transfer capacity and thus is suitable for photovoltaic (PV) applications. Primary device voltage is clamped at reflected output voltage, and secondary device voltage is clamped at output voltage. Steady-state operation and analysis, and design procedure are presented.

A zero-voltage-switching (ZVS) dc-dc converter with high voltage gain is proposed. It consists of a ZVS boost converter stage and a ZVS half-bridge converter stage and two stages are merged into a single stage. The ZVS boost converter stage provides a continuous input current and ZVS operation of the power switches. The ZVS half-bridge converter stage provides a high voltage gain. The principle of operation and system analysis are presented. Theoretical analysis and performance of the proposed converter were verified on a 100 W experimental prototype operating at 108 kHz switching frequency. During their commutations the resonant network operates for a very short period to create ZVS or ZCS conditions for the main semiconductors.

**INTRODUCTION:** Advances in resonant and quasi-resonant power conversion technology propose alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Currently, the conventional approaches are by far, still in the production mainstream. However, an increasing challenge can be witnessed by the emerging resonant technologies, primarily due to their lossless switching merits. The intent of this presentation is to umavel the details of zero voltage switching via a comprehensive analysis of the timing intervals and relevant voltage and current waveforms. The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by one individual [1] and publicized by another at various power conferences [2,3]. Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters [4,5,6,7,8]. In theory, the on off transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current, hence zero power switching. And while true, two obvious concerns can inl pede the quest for high efficiency operation with high voltage inputs. By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its square wave kin when activated by the next drive pulse, the MOSFET output capacitance (Coss) is discharged by the FET, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique.

# ZERO VOLTAGE SWITCHING OVERVIEW

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of tin1e, this method is similar to fIXed frequency conversion which uses an adjustable duty cycle, as shown in Fig. 1. Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency, changing the effective on-time in a ZVS design. The foundation of this conversion is sin1ply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly el unlike the energy transfer system of its electrical dual, the zero current switched converter. During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the volt - age across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (Coss) has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch. Therefore, the MOSFET transition losses go to zero -regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when V DS equals zero. The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few. This presentation will focus on the continuous output current, buck derived topologies, however a list of references describing the others has been included in the appendix.





## **ZVS BENEFITS**

- zero power " Lossless " switching transitions
- Reduced EMI / RFI at transitions
- No power loss due to discharging Coss
- No higher peak currents, (ie. ZCS) same as square wave systems
- High efficiency with high voltage inputs at any frequency
- Can incorporate parasitic circuit and compo
- Reduced gate drive requirements (no "Miller" effects)
- Short circuit tolerant

## **ZVS DIFFERENCES:**

- Variable frequency operation (in general)
- Higher off-state voltages in single switch, unclamped topologies
- Relatively new technology -users must climb the learning curve
- Conversion frequency is inversely proportional to load current
- A more sophisticated control circuit may be required

# **ZVS DESIGN EQUATIONS**

A zero voltage switched Buck regulator will be used to develop the design equations for the various voltages, currents and time intervals associated with each of the conversion periods which occur during one complete switching cycle. The circuit schematic, component references, and relevant polarities are shown in Fig. 4.Typical design procedure guidelines and "shortcuts" will be employed during the analysis' for the purpose of brevity. At the onset, all components will be treated as though they were ideal which simplifies the generation of the basic equations and relationships. As this section progresses, losses and non-ideal characteristics of the components will be added to the formulas. The timing summary will expound upon the equations for a precise analysis. Another valid assumption is that the output fIlter section consisting of output inductor Lo and capacitor Co has a time constant several orders of magnitude larger than any power conversion period. The fIlter inductance is large in comparison to that of the resonant inductor's value LR and the magnetizing current MLo as well as the inductor's DC resistance is negligible. In addition, both the input voltage VIN and output voltage Vo are purely DC, and do not vary during a given conversion cycle. Last, the converter is operating in a closed loop configuration which regulates the output voltage Vo.

## **INITIAL CONDITIONS:**

Time interval < to Before analyzing the individual time intervals, the initial conditions of the circuit must be deflDed. The analysis will begin with switch Ql on, conducting a drain current ID equal to the output current Io, and VDs = VCR = O (ideal).

In series with the switch Ql is the resonant inductor LR and the output inductor Lo which also conduct the output current Io .It has been established that the output inductance Lo is large in comparison to the resonant inductor LR and all components are ideal. Therefore, the voltage across the output inductor V Lo equals the input to output voltage differential; V Lo = VlN -Vo .The output filter section catch diode Do is not conducting and sees a reverse voltage equal to the input voltage; V Do = Vl, observing the polarity shown in Figure 4.

COMP	STATUS	CIRCUIT VALUES
01	ON	VDS=VCR=O;
		ID=ILR=ILO=lo
Do	OFF	VDO=VIN; IDO=O
LA		I LR=IO ; VLR=O
Lo		V, r)=VIN-VO ; ILO=O

#### Table I. INITIAL CONDITIONS

## CAPACITOR CHARGING STATE: t0 -t1

The conversion period is initiated at time to when switch QI is turned OFF. Since the current through resonant inductor LR and output inductor Lo cannot change instantaneously, and no drain current flows in QI while it is off, the current is diverted around the switch through the resonant capacitor CR. The constant output current will linearly increase the voltage across the resonant capacitor until it reaches the input voltage (V CR = v IN). Since the current is not changing, neither is the voltage across resonant inductor LR. At time to the switch current ID "instantly" drops from 10 to zero. Simultaneously, the resonant capacitor current IcR snaps from zero to 10, while the resonant inductor current ILR and output inductor current ILO are constant and also equal to 10 during interval tOr .Voltage across resonant capacitor CR. At time t1' V CR equals V IN' and Do starts to conduct.



It is off, the current is diverted around the switch through the resonant capacitor CR. The constant output current will linearly increase the voltage across the resonant capacitor until it reaches the input voltage (V CR = v IN). Since the current is not changing, neither is the voltage across resonant inductor LR. At time to the switch current ID "instantly" drops from 10 to zero. Simultaneously, the resonant capacitor current IcR snaps from zero to 10, while the resonant inductor current ILR and output inductor current ILO are constant and also equal to 10 during interval tor. Voltage across resonant capacitor CR. At time t1' V CR equals V IN' and Do starts to conduct.

# Table II - CAPACITOR CHARGING: t<sub>0</sub> - t<sub>1</sub>

COMP.	STATUS	CIRCUIT VALUES
Q <sub>1</sub>	OFF	$I_{D} = 0$ ; $V_{DS(t)} = V_{CR(t)}$
C <sub>R</sub>	Chargin <b>g</b>	I <sub>CR</sub> =0 ; V <sub>CR(t)</sub> RISES LINEARLY V <sub>CR(t0)</sub> =0 ; V <sub>CR(t1)</sub> ≢V <sub>IN</sub>
L <sub>R</sub>		$I_{LR(t)} = I_{O}; V_{LR} = 0$
D <sub>O</sub>	OFF	V <sub>DO(t0)</sub> = V <sub>IN</sub> ; V <sub>DO(t1)</sub> = 0 ; DECREASES LINEARLY
ե		$V_{LO(t0)} = V_{IN} V_0$ ; $V_{LO(t1)} = V_0$ DECREASES LINEARLY; $I_{LO} = I_0$

# **RESONANT STATE: tl -t2**

The resonant portion of the conversion cycle begins at t 1 when the voltage across resonant capacitor V CR equals the input voltage V IN' and the output catch diode begins conducting- At t I, current through the resonant components IcR and ILR equals the output current 10. The stimulus for this series resonant L-C circuit is output current 10 flowing through the resonant inductor prior to time ti. The ensuing resonant tank current follows a cosine function beginning at time ti' and ending at time t2- At the natural resonant frequency "R, each of the L-G tank components exhibit an impedance equal to the tank impedance, ZR-Therefore, the peak voltage across GR and switch Ql are a function of ZR and 10. The instantaneous voltage across GR and Ql can be evaluated over the resonant time interval using the following relationships:

$$V_{CR(t)} = V_{CR(t)} + \frac{I_o}{\omega_R C_R} \sin[\omega_R(t-t_1)]_{t_1}^{t_2}$$

$$Z_R = 1/\omega_R C_R \qquad V_{CR(t)} = V_{IN}$$

$$\therefore \quad V_{CR(t)} = V_{IN} + I_o Z_R \sin[\omega_R(t-t_1)]_{t_1}^{t_2}$$

Of greater importance is the ability to solve the equations for the precise off-time of the switch. This off-time will vary with line and load changes and the control circuit must respond in order to facilitate true zero voltage switching. While some allowance does exist for a fIXed off time technique, the degree of latitude is insufficient to accommodate typical input and output variations. The exact time is obtained by solving the resonant capacitor voltage equations for the condition when zero voltage is attained.

Let 
$$V_{CR(t)} = 0$$
;  $I_0 Z_R SIN(\omega_R(t-t_1)) = -V_{IN}$ 

The resonant component current (IcR = ILR) is a cosine function between time t 1 and t2' described as:

$$I_{CR(t)} = I_0 \cos \left[ \omega_R (t-t_1) \right]_{t_1}^{t_2}$$

The absolute maximum duration for this interval occurs when 270 degrees (311" /2UJ~ of resonant operation is required to intersect the zero voltage axis. This corresponds to the limit of resonance as minimum load and maximum line voltage are approached. Contributions of line and load influences on the resonant time interval t]2 can be analyzed individually as shown in Figs. 7 and 8. Prior to time tl' the catch diode Do was non conducting. Its voltage, V 00' was linearly decreasing from V IN at time to to zero at ti while input source V IN was supplying full output current, Io. At time tl' however, this situation changes as the resonant capacitor initiates resonance, diverting the resonant inductor current away from the output filter section Instantly, the output diode voltage, V 00' changes polarity as it begins to conduct, supplementing the decreasing resonant inductor current with diode current loo. Extracted from store energy in output inductor Loo The diode current wave shape follows a cosine function during this interval, equalling Io minus IcR(t). Also occurring at time tl' the output filter inductor Lo releases the stored energy required



Fig. 8 -Resonant Capacitor Voltage vs. Load to maintain a constant output current 10. Its reverse voltage is clamped to the output voltage Vo minus the diode voltage drop V DO by the convention followed by Figure 4.

**INDUCTOR CHARGING STATE: t2 -t3:** To facilitate zero voltage switching, switch Ql is activated once the voltage VD S across Ql and resonant capacitor V CRh as reached zero, occurring at time t2. During this inductor charging interval tv resonant

inductor current I LR is linearly returned from its negative peak of minus 10 to its positive level of plus 10. The output catch diode D 0 conducts during the t2J interval- It continues to freewheel the full output current 10, clamping one end of the resonant inductor to ground through D 0- There is a constant voltage, VIN -V DO, across the resonant inductor. As a result, ILR rises linearly, 100 decreases linearly. Energy stored in output inductor Lo continues to be delivered to the load during this time period. A note worthy peculiarity during this timespan can be seen in the switch drain current waveform. At time t2' when the switch is turned on, current is actually returning from the resonant tank to the input source, VIN- This indicates the requirement for a reverse polarity diode across the switch to accommodate the bidirectional current. An interesting result is that the switch can be turned on at any time during the first half of the t2Ji nterval without affecting normal operation. A separate time interval could be used to identify this region if desired.

 $\frac{dI_R}{dt} = \frac{V_{IN}}{L_R} ; dt = dI_R L_R / V_{IN}$  $t_{23} = \frac{L_R \Delta I_R}{V_{IN}}$ 

where  $\Delta I_R = -I_0$  to  $+I_0 = 2I_0$ 

$$\frac{L_R I_O}{V_{in}}$$
 and varies with  $V_{in}$  and  $V_O$ 

Table IV - INDUCTOR CHARGING: t2 - t3

COMP.	STATUS	CIRCUIT VALUES
Q,	ON	$I_{D(t)} = -I_{O} + ((V_{IN} + V_{DO})/L_{R})t$
CR		V <sub>CR</sub> =0
L <sub>R</sub>	Charging	$V_{LR} = V_{IN} + V_{DO}$ $I_{LR(t)} = -I_O + (V_{LR}/L_R)(t-t2)$
Do	ON	DO(1) = 10-1LA(1)
L <u>o</u>		$I_{LO} = I_O ; V_{LO} = -(V_O + V_{DO})$

**POWER TRANSFER STATE: t3 -t4:** Once the resonant inductor current ILR has reached 10 at time tj, the zero voltage switched converter resembles a conventional square wave power processor. During the remainder of the conversion period, most of the pertinent waveforms approach DC conditions. Assuming ideal components, with QJ closed, the input source supplies output current, and the output filter inductor voltage V LO equals VIN -V 0. The switch current and resonant inductor current are both equal to 10, and their respective voltage drops are zero (VDs=VLR=O). Catch diode voltage V DO equals VIN, and IDO=O.

In closed loop operation where the output voltage is in regulation, the control circuit essentially varies the on-time of the switch during the tJ4 interval. Variable frequency operation is actually the result of modulating the on-time as dictated by line and load conditions. Increasing the time duration, or lowering the conversion frequency has the same effect as widening the duty cycle in a traditional square wave converter. For example, if the output voltage were to drop in response to an increased load, the conversion frequency would decrease in order to raise the effective ON period. Conversely, at light loads where little energy is drawn from the output capacitor, the control circuit would adjust to minimize the tJ4 duration by increasing the conversion frequency. In summary, the conversion frequency is inversely proportional to the power delivered to the load

$$V_{O} = \frac{V_{IN}t_{34}}{t_{01}+t_{12}+t_{23}+t_{34}} = \frac{V_{IN}t_{34}}{t_{03}+t_{34}}$$

$$t_{34} = \frac{V_{O}t_{03}}{V_{IN}-V_{O}}$$

$$T_{A} = \frac{V_{O}t_{03}}{V_{IN}-V_{O}}$$

$$T_{A} = \frac{V_{O}t_{03}}{V_{IN}-V_{O}}$$

$$T_{A} = \frac{V_{O}t_{03}}{V_{IN}-V_{O}}$$

$$T_{A} = \frac{V_{O}t_{03}}{V_{O}+V_{O}}$$

$$T_{A} = \frac{V_{O}t_{03}}{V_{O}+V_{O}}$$

$$T_{A} = \frac{V_{O}t_{03}}{V_{O}+V_{O}}$$



**CONCLUSION:** The zero voltage switched quasi-resonant technique is applicable to most power conversion designs, but is most advantageous to those operating from a high voltage input. In these applications, losses associated with discharging of the MOSFET output capacitance can be significant at high switching frequencies, impairing efficiency. Zero voltage switching avoids this penalty by negating the drain-to-source, "off-state" voltage via the resonant tankA high peak voltage stress occurs across the switch during resonance in the buck regulator and single switch forward converters. Limiting this excursion demands limiting the useful load range of the converter as well, an unacceptable solution in certain applications. For these situations, the zero voltage switched multi-resonant approach [14,15] could prove more beneficial than the quasi-resonant ZVS variety. Significant improvements in efficiency can be obtained in high voltage to the input rails avoids the high voltage overshoot concerns of the single switch converters, while transforD1er reset is accomplished by the bidirectional switching. Additionally, the series transforD1er primary and circuit inductances can beneficial, additives in the formation of the total resonant inductor value. This not only reduces size, but incorporates the detrimental parasitic generally snubbed in square wave designs, further enhancing efficiency.



Fig : zero voltage switching converter

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