

Design a Simulation an Asymmetrical 11-Level Inverter for Photovoltaic Applications

¹Priyanka Salwe, ²Prof. Priyanka Dukare

¹PG Student, ²Assistant Professor
Department of Electrical Engineering
Abha Gaikwad Patil College of Engineering, Nagpur

Abstract: Increasing demands of power conversion technology encourages multilevel converters emerge as a solution to overcome limitations at power ratings in conventional methods of power converters. This paper discusses about a new asymmetrical construction of an 11-level inverter, despite the focus on the following design, few comparisons of the conventional topological construction will be stated. Limitations in conventional types topologies often deals with its complexity and volume. It will be furthered mentioned how the asymmetrical topology of the 11-level inverter design deals and overcome these limitations and reduce harmonic distortions for grid-tied PV systems. The proposed construction is designed and simulated by MATLAB software. Analysis of Real-Time Simulation of the proposed design results in a THD value.

Keywords: 11 Level Multilevel Inverter, Photovoltaic, PWM, Swithing Sequence, MATLAB.

I INTRODUCTION

Power electronics are the core of modern application conversion systems. The increasing demands to improve efficiency, usage flexibility leads to technical challenges around the control method used and their topologies. Multilevel inverters could overcome the power ratings and handling limits by shared through ratings in the components of the switches. These converter trends are largely applied to renewable technologies and industry appliances. As the output of the PV cells are DC, and after maximizing the DC power output by the MPPT. DC power is converted to AC as a source for home and industrial appliances. Conventional constructions of inverters are limited by their components power ratings. As a result, methods of multilevel conversion are used to share and distribute power collective through the components. Most commonly known topologies are the flying capacitor and diode-clamp constructions. But as levels are increased these builds up volume, cost and number of switches. Asymmetrical design generally satisfies this objective and with the increased levels, harmonic distortions which percentage nominal that are regulated by IEEE standards in output power are reduced.

Advantages of the construction increases demands of smaller, efficient, rigid types of multilevel inverters in time, resulting in reduced number of switches and maximizing their potential in distributed power. As these are the trends in modern usage power conversion multilevel inverter design. In response to the conventional limitations of inverters, this paper proposes a new asymmetrical 11-level inverter design, simulated with MATLAB. It will be stated the recommended practices for harmonic values by IEEE and could be considered how harmonic values in inverter design could be implemented in different types of applications. Even after implementing

multilevel topologies (e.g diode clamp, flying capacitor, isolated power sources), the limits of the topology will cover around the number of switches used and switching operations that will affect effectiveness in further PV applications. The paper will also cover how the proposed 11-level inverter design would be capable to overcome conventional topology problems by the effective reduced number of switches to achieve a high number of n-levels and how this design could be useful to further research in higher n-level applications to reduce harmonic values even lower.

II. MULTILEVEL INVERTER CIRCUIT.

A Multilevel Inverter is created [18] by cascading two three-phase three-level inverters using the load connection, with only one dc voltage source, that can operate as a seven-level inverter and naturally splits the power conversion into a higher-voltage lower-frequency inverter and a lower-voltage higher-frequency inverter. Two types of control: controlling the two three-level inverters jointly and separately, are developed that included capacitor voltage balancing so that a dc source was needed for only one three-level inverter. A survey presents different topologies, control strategies and modulation techniques used by multilevel inverters. Regenerative and advanced topologies are also discussed. Finally, applications and future developments are addressed. Cascaded multilevel inverter have evolved from a theoretical concept to real applications due to high degree of modularity, possibility of connecting directly to medium voltage, high power quality, high availability, and the control of power flow in the regenerative version. Power quality improvement with proposed filter has been verified by the simulation results with MATLAB/SIMULINK. Multilevel inverter based shunt APF is found to inject the compensating current, hereby reduces the magnitude of the significant harmonics in the line current and hence the Total Harmonic Distortion.

The N-level cascaded H-bridge, multilevel inverter comprises series connected single phase H-bridges per phase, for which each H-bridge has its own isolated dc source.

Fig1. Shows one phase of a n-level cascaded H-bridge inverter. The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each H-bridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches. Its main limitation lies in its need for isolated power sources for each level and for each phase, although for VA compensation, capacitors replace the dc supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive feature.

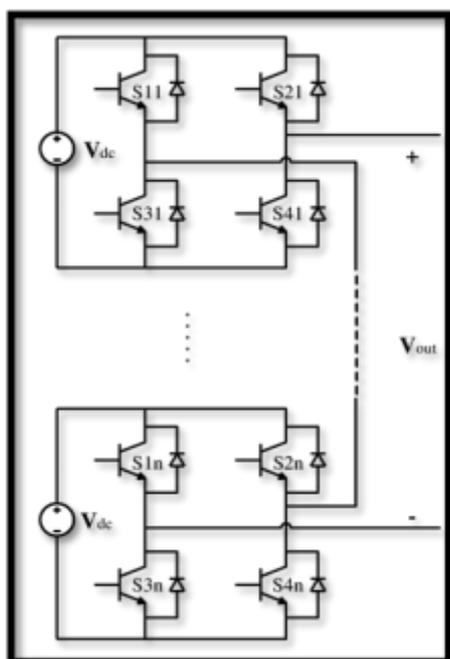


Fig.1 Conventional Cascaded Multilevel Inverter

algorithms imagine a steady sampling interval of the control, T_s .

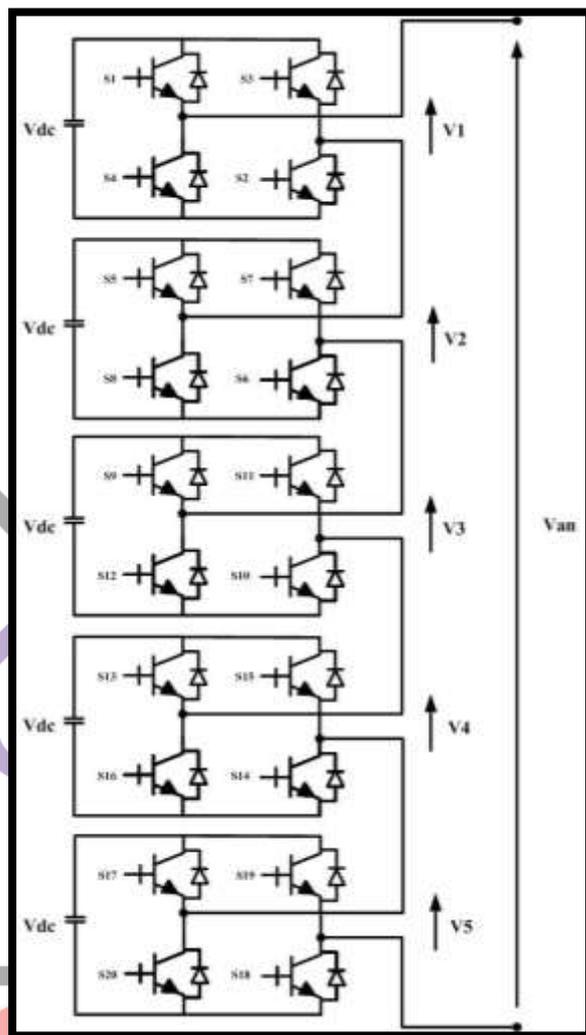


Fig.3 Proposed Multilevel Inverter.

A. General Description.

In multilevel inverters with a fundamental frequency switching strategy, the switching angles can be selected so that the output THD is minimized. The output voltage will have fundamental and the associated harmonics. These harmonics produce additional heating in the system, when the output voltage of the inverter is fed to the load. Therefore in order to reduce the losses in the form of heat, harmonics reduction is necessary.

Fig.2 explains the block diagrams of existing system. 7 dc sources are used. Battery act as a DC sources. This DC input is given to the three phase multilevel inverter circuit and the inverter converts DC in to AC. For triggering the switches present in the inverter circuit, square wave pulses are given to the multilevel inverter Circuit. The output of the inverter is given to the AC load.

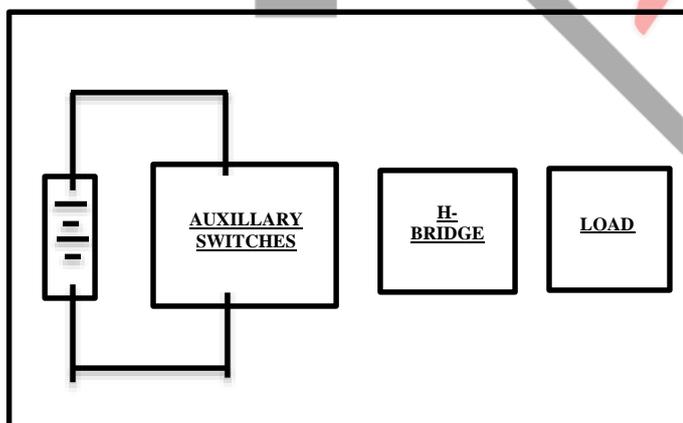


Fig.2 Block Diagram.

The first one uses a stable switching state during a full sampling interval (step or staircase method), whereas the second one is implemented with a Pulse Width Modulation (PWM method). Both methods receive that the DC source voltages are not steady but variable in time. The definite voltages on the capacitors are therefore calculated, and the phase voltage vector V_{ii} is created. In order to compute all attainable output voltages V_{ol} , the phase voltage vector is multiplied with all possible switching states S_i . This results in an unsorted vector containing all feasible output voltages.

This inverter having 20 bridges connected in series gives different levels of output voltages without changing the circuit except the ratios of input voltages. Switching of the converter is done by following the staircase control technique. Pulse width Modulation technique can also be applied by appropriate calculation of the switching time period.

III. PROPOSED MULTILEVEL INVERTER

A converter consisting of twenty modules with a DC Sources will result in huge number of diverse output voltage levels. This composition will be compared with the predictable approach with identical DC voltage sources. Two different control methods for a single phase converter are offered. Both

B. Switching Sequence

An innovative and quintessential PWM modulation technique has been introduced into this literature for the generation of PWM switching signals in the proposed eleven level inverter, from several decades, the shifted amplitude sinusoidal PWM is a very common strategy in the multilevel inverter topology. In this paper a very distinctive and unique

switching technology has been introduced, a photovoltaic source is given to the each switching circuit as compared to Vdc voltage source or we can say that this 11 level multilevel inverter is used for PV application. Due to this Switching technic the fluctuation in voltage is not happens when we use PV.

Switches Turn ON	Voltage Level
S1,S2,S5,S6,S9,S10,S13,S14,S17,S18	5Vdc
S1,S2,S5,S6,S9,S10,S13,S14,S18,S20	4Vdc
S1,S2,S5,S6,S9,S10,S14,S16,S18,S20	3Vdc
S1,S2,S5,S6,S10,S12,S14,S16,S18,S20	2Vdc
S1,S2,S6,S8,S10,S12,S14,S16,S18,S20	Vdc
S2,S4,S6,S8,S10,S12,S14,S16,S18,S20	0
S3,S4,S6,S8,S10,S12,S14,S16,S18,S20	-Vdc
S3,S4,S7,S8,S10,S12,S14,S16,S18,S20	-2Vdc
S3,S4,S7,S8,S11,S12,S14,S16,S18,S20	-3Vdc
S3,S4,S7,S8,S11,S12,S15,S16,S18,S20	-4Vdc
S3,S4,S7,S8,S11,S12,S15,S16,S19,S20	-5Vdc

Table.1 Switching Sequence.

There is some Mode's which is given below, from which we can able to understand the working of system.

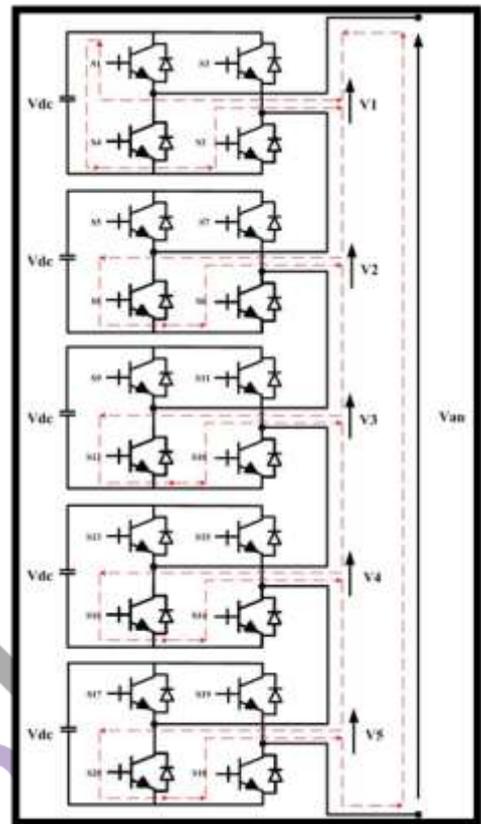


Fig.5 Mode 1 (Vdc)

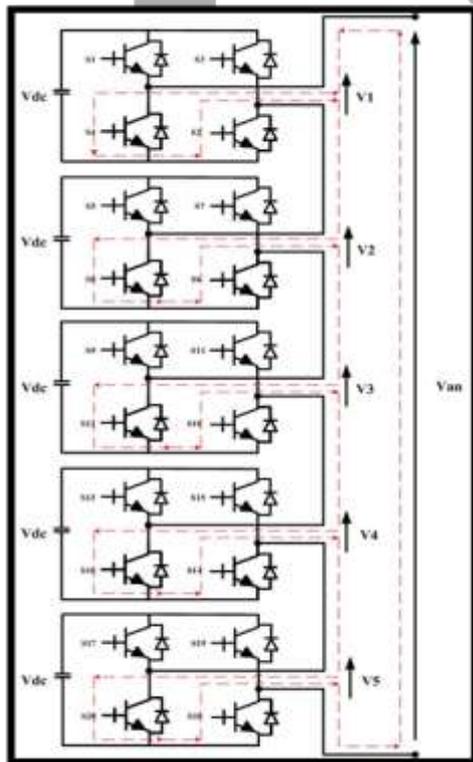


Fig.4 Mode 0

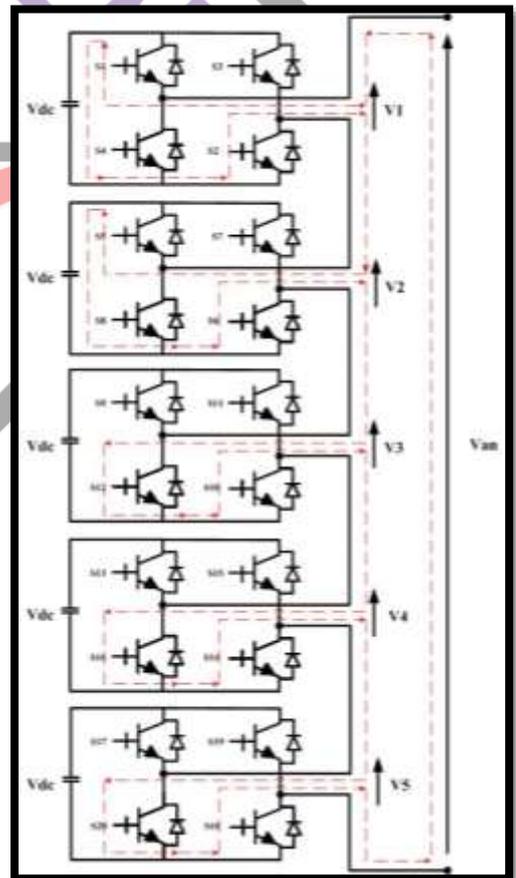


Fig.6 Mode 2 (2Vdc)

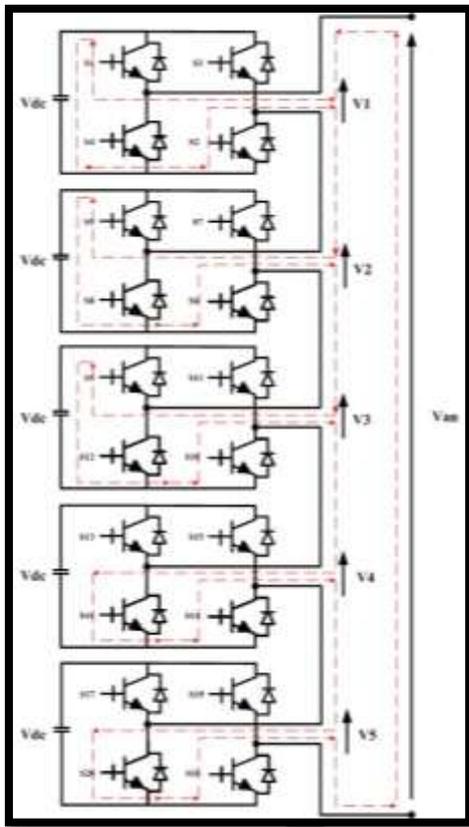


Fig.7 Mode 3 (3Vdc)

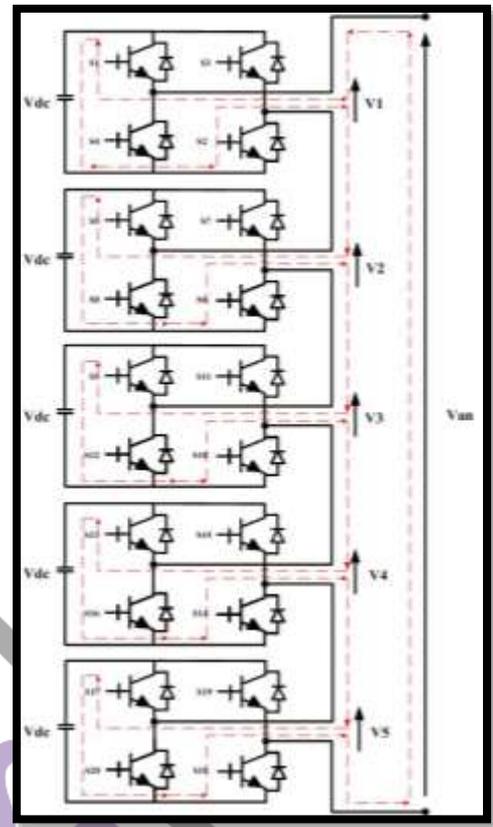


Fig.9 Mode 5 (5Vdc)

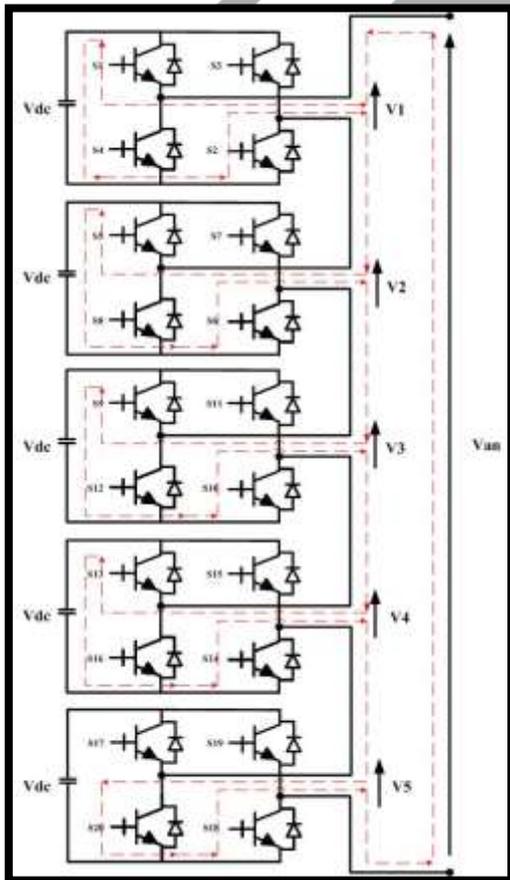


Fig.8 Mode 4 (4Vdc)

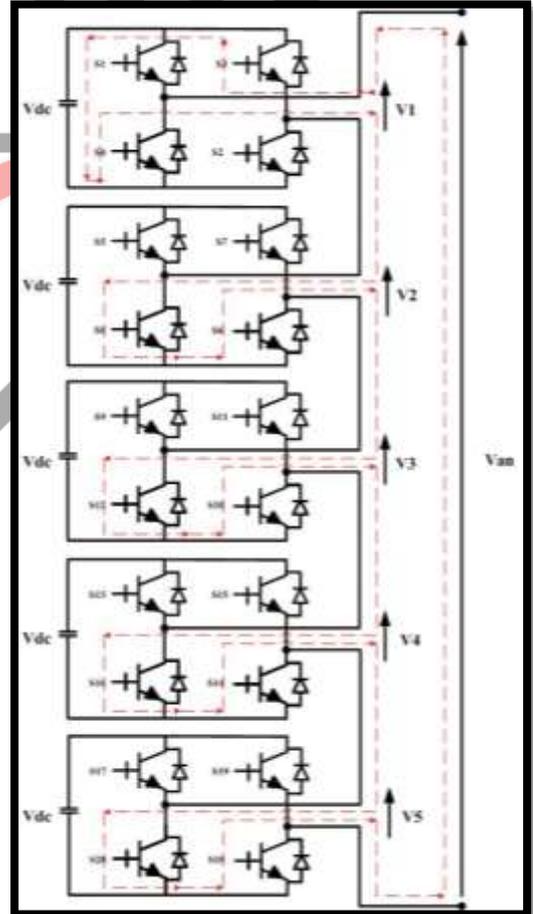


Fig.10 Mode 6 (-1Vdc)

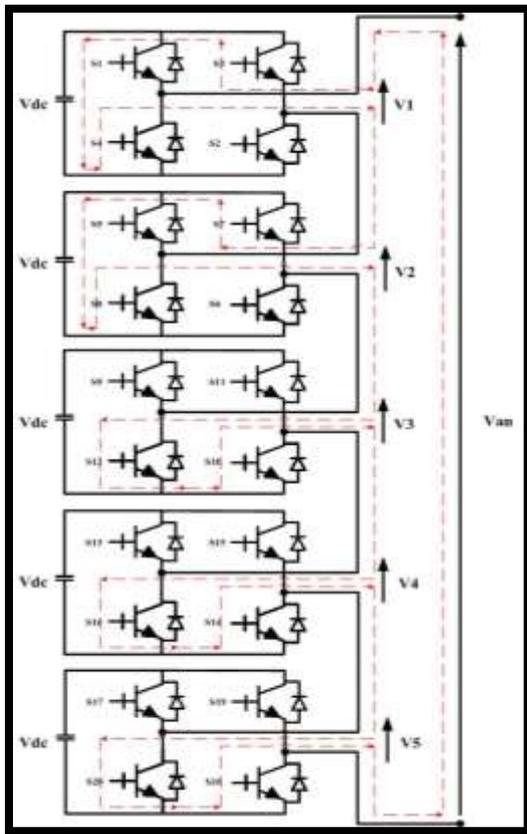


Fig.11 Mode 7 (-2Vdc)

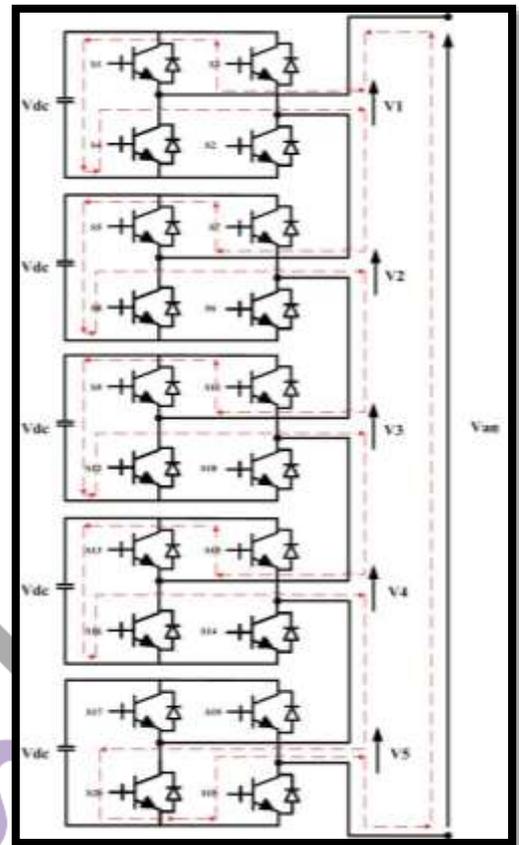


Fig.13 Mode 9 (-4Vdc)

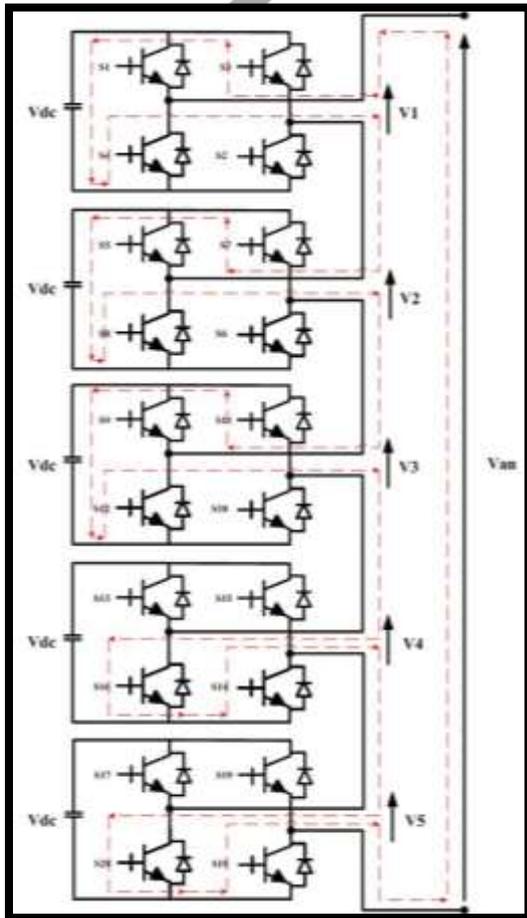


Fig.12 Mode 8 (-3Vdc)

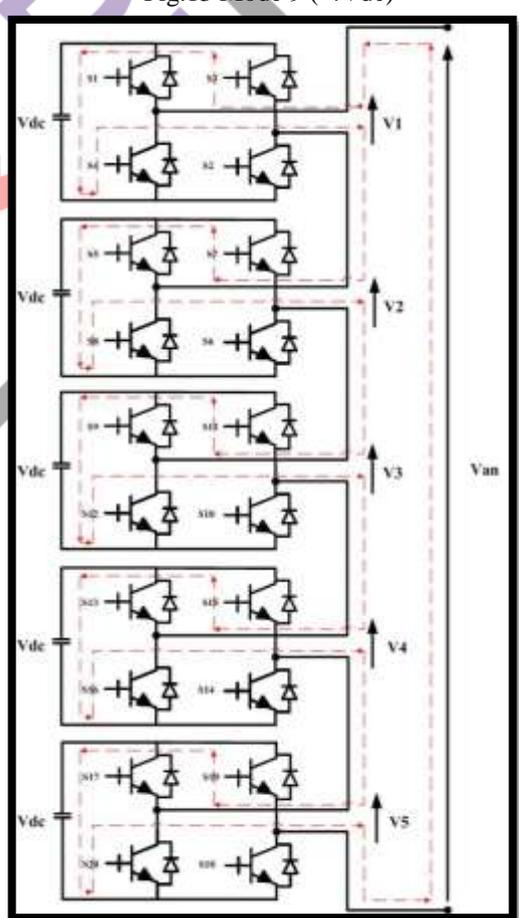


Fig.14 Mode 10 (-5Vdc)

IV. SIMULATION RESULT

The simulation case study has been carried out software to validate the result. Fig.16. Shows the simulation model of the proposed topology. To generate the 11- level output voltage, 20 IGBTs and five DC power source which come from the PV system. Pulses are generated by using nearest level control method. The simulated Output voltage is shown in Fig.15. and the harmonic spectrum was analyzed using the FFT Window in MATLAB/Simulink.

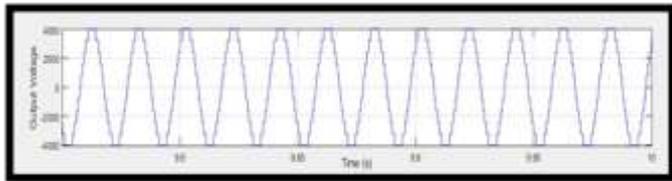


Fig.15 Output Voltage

The 11 level inverter output is shown in Fig.15. It has 11 levels of voltages in a half cycle and because of the unequal step widths, it resembles much more to a sine wave. As a result, the harmonic spectrum of the output will be improved. The FFT analysis of the output voltage waveform must be carried out to find the THD of the output voltage waveform.

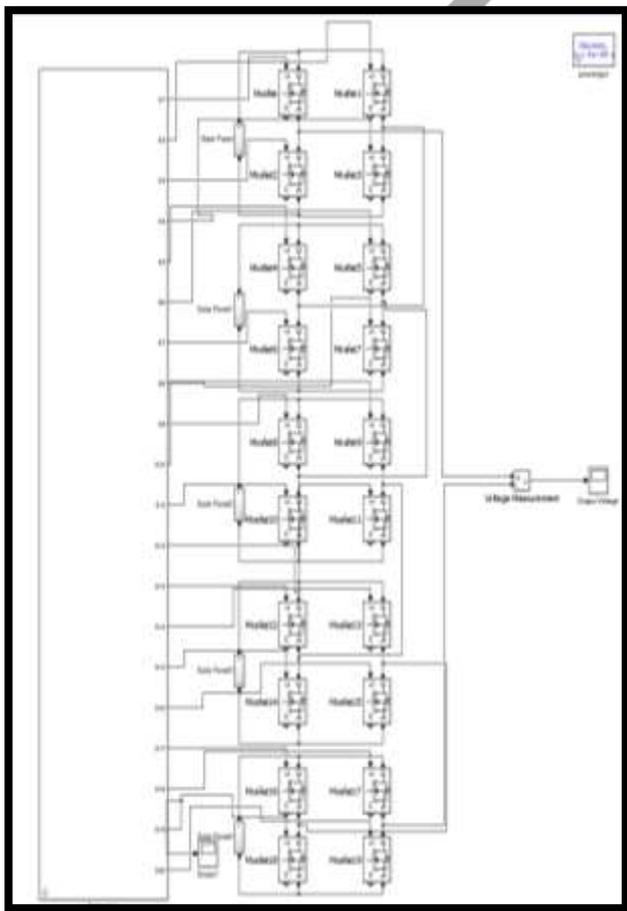


Fig.16 Simulation model of the proposed inverter.

V. CONCLUSION

This paper has covered mainly in the proposed design for the asymmetrical 11-level inverter for PV application by applying the DC voltage source from the PV and controlling

the fluctuation in source voltage by the different switching modes.

The THD value for this design analyzed and observed by Real-Time simulation MATLAB software by simulation model is 3.45% which is within range of IEEE standards 5% for harmonic voltage limits for power producers.

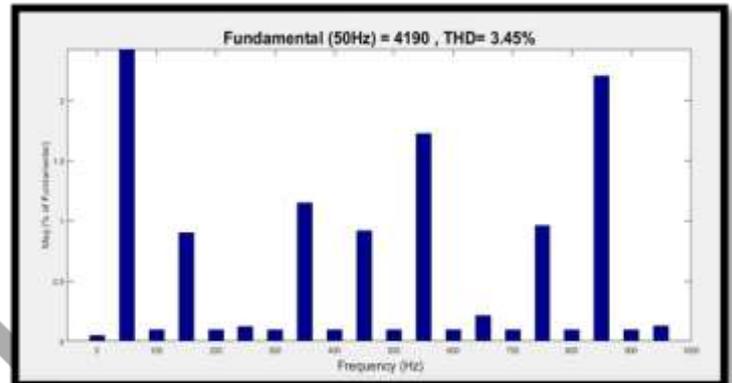


Fig.17 FFT Analysis Of Output Voltage.

REFERENCES

- [1] Christopher Tjokro, Leonardus H. Pratomo,(2018) Design and Simulation of an Asymmetrical 11-Level Inverter for Photovoltaic Systems ICITACEE.
- [2] Sixing, D., Dekka, A., Wu, B., & Zargari, N. (2018). Modular Multilevel Converters. IEEE Press
- [3] Kahwa, A., Obara, H., & Fujimoto, Y. (2018). Design of 5- level Reduced Switches Count H-bridge Multilevel Inverter
- [4] Wira Adhitama Cahyosaputro , Leonardus Heru, A Single Phase 11-Level Inverter for Photovoltaic Application, 2018 5th Int. Conf. on Information Tech., Computer, and Electrical Engineering (ICITACEE)
- [5] Rashid, M. H. (2016). Alternative Energy in Power Electronics
- [6] Sochor, P., & Akagi, H. (2016). Theoretical comparison in energy-balancing capability between star- and delta configured modular multilevel cascade inverters for utility scale photovoltaic systems. IEEE Transactions on Power Electronics, 31(3), 19801992
- [7] Rashid, M. H. (2016). Alternative Energy in Power Electronics.
- [8] Kahwa, A., Obara, H., & Fujimoto, Y. (2018). Design of 5-level Reduced Switches Count H-bridge Multilevel Inverter.
- [9] Pratomo, L. H., Wijaya, F. D., & Firmansyah, E. (2015). Capacitor Bank Voltage Equilibrium for MPPT in Single-Phase Single-Stage Five-Level Inverter for PV-Grid Application. TELKOMNIKA Indonesian Journal of Electrical Engineering, 14(1), 6271. <https://doi.org/10.11591/telkomnika.v14i1.764>
- [10] Bhaskar, M. S., Padmanaban, S., Fedk, V., Blaabjerg, F., & Wheeler, P. (2017). Transistor clamped five-level inverter using non-inverting double reference single carrier PWM technique for photovoltaic applications. Proceedings - 2017 International Conference on Optimization of Electrical and Electronic Equipment, OPTIM 2017 and 2017 Intl Aegean Conference on Electrical Machines and Power Electronics, ACEMP 2017, (c), 777782. <https://doi.org/10.1109/OPTIM.2017.7975063>

- [11] Nagar, S., Khan, S., & Singh, B. (n.d.). Performance of Cascaded Diode Bridge Integrated H- Bridge 13 Level Multilevel Inverter, 3, 37.
- [12] S. A. Amamra, K. Meghriche, A. Cherifi, and B. Francois. Multilevel inverter topology for renewable energy grid integration. IEEE Transactions on Industrial Electronics, 64(11):8855–8866, Nov 2017.
- [13] N. Prabakaran and K. Palanisamy. Analysis of cascaded h-bridge multilevel inverter configuration with double level circuit. IET Power Electronics, 10(9):1023–1033, 2017.
- [14] S. R. Raman, K. W. E. Cheng, and J. Hu. A seven level switched capacitor multilevel inverter with asymmetric input sources for microgrids. In 2017 20th International Conference on Electrical Machines and Systems
- [15] S. K. Sahoo and T. Bhattacharya. Phase-shifted carrier-based synchronized sinusoidal pwm techniques for a cascaded h-bridge multilevel inverter. IEEE Transactions on Power Electronics, 33(1):513–524, Jan 2018.

