Low power FinFET SRAM design and analysis using leakage current reduction techniques

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Abstract- **This paper looks at creating a low-power FINFET SRAM and using various methods to cut down on leakage current. Because they may be scaled, the CMOS parameters are not giving lower technology nodes trustworthy values. In an effort to lessen the detrimental effects of MOSFET scaling, researchers are searching for solutions, and FINFET has surfaced as one of the greatest alternatives since it offers superior performance characteristics, such as reduced energy consumption, the removal of short-channel effects, and improved gate control lowers the leakage current in the sub-32 nm range. Since a significant increase in battery-operated portable devices has occurred, electronic devices need to be used for extended periods of time after the battery is fully charged. In order to accomplish this, the gadget should have reduced leakage current. This will allow it to function for extended periods of time with the least amount of leakage power feasible. First, all the parameters were computed and a 6-T CMOS SRAM was designed. The development of DG-FINFET SRAM followed, and all the parameters were computed. Compared to the 6 T SRAM designed using CMOS, the FinFET-based 6 T cell architecture uses a significant amount less power. It has been discovered that SRAM cells have less leakage power than conventional SRAM due to the application of numerous leakage current reduction strategies in FinFET SRAM.**

Index terms: **FINFET, SRAM, CMOS, leakage current, leakage power etc.**

I. INTRODUCTION

The MOS technology has led to a rapid expansion of the semiconductor industry [1]. The extension of CMOS technology beyond the nanometer scale is fraught with challenges. Numerous difficulties arise with scalability, such as increased production costs, decreased reliability, increased power consumption, and significant parameter changes. Scalability issues cause CMOS properties to deteriorate at lower technological nodes. The FINFET has been found to be one of the finest MOSFET substitutes since it consumes less energy, has no short channel effects, and lowers leakage current. Although power consumption was decreased, CMOS efficiency was severely decreased [2]. This can be accomplished by reducing its oxide thickness. At the expense of better gate channel control, this leads to a higher current [3]. When one parameter is increased, another's efficacy drops. Researchers are looking for metal gate electrodes to replace polysilicon because of the possibility of thermal instability [4].Nevertheless, it was found that metal gates operated in an inefficient manner. Therefore, it is highly likely that alternative transistor architectures like the Field Effect Transistor (FET), Ultra-thin Body (UTB), Fin Field Effect Transistor (FinFET), and Double-Gate Metal Oxide Semiconductor Field Effect Transistor (DG MOSFET) will have to be used in order to continue gate length scaling down to the sub-32 nm regime [5].

At the nanoscale, FinFETs have been demonstrated to be the most effective bulk CMOS alternatives due to their double gate, which allows for improved channel regulation. Similar gates can be shorted to boost efficiency or regulated individually to lower the number of transistors or leakage current. There are two varieties of double gate FinFETs that can be utilized: independent gate FinFETs (IG) and short-circuit gates (SG). The SG FinFET can be entered or exited by connecting the two gates on either side. Narrow fins are used in the core of the FinFET design to help channel current, lower SCE, and produce less heat. Short-channel effects can be lessened by using fin-FETs with multiple gates [6]. The gate insulator width limits the lowering of FinFET gate channel lengths [7]. Reducing the power supply is also necessary to reach a steady performance threshold.

Complementary metal oxide semiconductors (CMOS) were used in the design of memory cells, but at lower technological nodes. Gate-Induced Barrier Lowering (GIBL) and sub-threshold leakage current are two of the various issues associated with CMOS technology that can be resolved with FinFET technology [1]. FinFETs can utilize technology knots as thin as 7 nm without sacrificing conducting capabilities, while bulk CMOS devices are restricted by limited channel widths of fewer than 45 nm. Memory design must make use of the nano range since most devices are built in this range [2]. Furthermore, FinFETs take the place of MOSFETs in order to address every issue [3]. For an error-free read operation, the read-out path, threshold voltage, and stacking scheme of the memory cell can minimize leakage [4].Figure 1 compares the structures of a FinFET with a conventional FET.

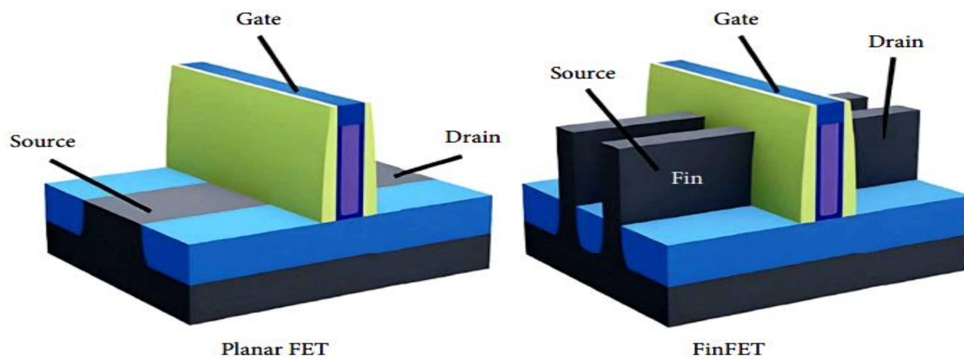


Figure 1: Structural comparison between FinFET and conventional FET

FinFET technology enhances controllability of low voltage operations by adding a second gate across the conventional gate.For FinFET to work, both gates must be present [5]. The Shorted-Gate (SG) mode is reached when these gates approach equal potential. Independent-Gate (IG) FinFETs are four terminal devices having physical isolation between gates, as opposed to shorted-gate (SG) FinFETs, which are three terminal devices. The flexibility of IG FinFET is more than that of SG FinFET. Figure 2 shows a two-dimensional perspective of FinFETs.

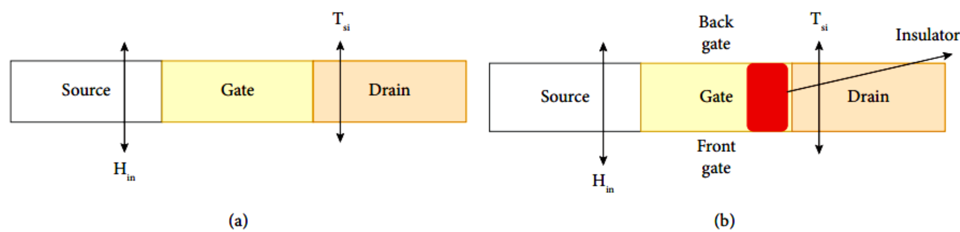


Figure 2: Description of FinFET (a) SG-FinFET (b) IG-FinFET

When two gates have different voltages, an IG FinFET operates. The other gate is used for switching devices and regulates the transistor's threshold voltage [6–8]. Quantized width (W) and H_{fin} are the different height elements of a fin [9, 10]. Equations (1) and (2) can be used to determine the quantization width of an SG FinFET and an IG FinFET respectively.

$$W_{SG} = 2 * H_{fin} + T_{si} \quad (1)$$

$$W_{IG} = 2 * H_{fin} \quad (2)$$

The fin thickness (T_{si}) can be discarded when computing the quantization width of IG FinFETs. In order to increase the width of the device, the total number of fins is increased in both cases. This paper illustrates the FinFET structure from the device level to the architecture level, as seen in Figure 3.

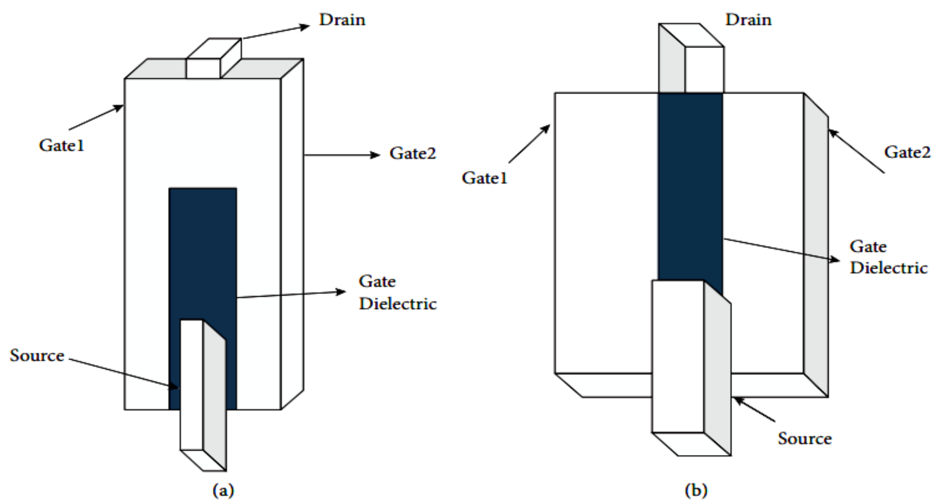


Figure 3: Two Dimensional Representation of FinFET (a) SG-FinFET (b) IG-FinFET

II. LITERATURE REVIEW

The present day 5G networks require high data rate for transmission of signal which consumes a lot of power, even the 5G network introduces IOT concept through which all the devices are connected with mobile networks. In order to achieve this wireless sensor networks are used which are low power consuming and cost effective and also in miniature

size. For the data transmission in such a way wireless sensor networks are established by spacing all the networks close to each other in large numbers. These networks have to work with low power consumption for which routing protocols are built which uses SRAM for data storage [19].

SRAMs are an important embedded part of the memory in any portable device. The SRAMs have become an integral part of the present-day memories as the device size is decreasing. Specifically, in biomedical applications like wireless body area networks, the low power SRAMs are an emerging trend. Since it is required to have low power devices reduction in power is the main criterion for any kind of VLSI device and it can be done by reducing the size and also the supply voltages. There appears to be not at all feasible alternatives of remaining out using the conventional MOSFET with down scaling from 65nm to 45nm or further smaller nodes. Rigorous Short Channel Effects (SCE) like Drain Induced Barrier Lowering (DIBL), Vth roll off, rising leakage currents like sub threshold S/D leakage, hot carrier effects and gate direct tunneling leakage that effect in device performance degradation are afflicting the industry [20].

Dropping the VDD helps decrease hot carrier effects and power however deteriorates the performance, which can be enhanced by dropping Vth but it degrades Source/ Drain leakage. To rise suitable gate control over channel and decline DIBL, the oxide width can be decreased but this augments the gate leakage. Resolving one problem directs to another. The improving of high gate dielectric to lessen the gate leakage and sufficient channel control is to be found out. But unfortunately, this investigation has not been successful to be used. There are band alignment problems (w.r.t Si) and/or interface states (with Si) and/or thermal instability. The current uncertainty crisis has led the scientists to search for metal gate conductors instead of poly-silicon. But metal gates conductors with opposed work resolutions haven‘t been initiated to be practical. Under this situation, poly-silicon remains to be used, where the work utility stresses that V_{th} be sited by high channel doping. Definitely, it is felt that as a substitute of planar MOSFETs. The alternate way is to use multi-gated devices and other devices made with different type of materials, and also a FinFET device. when the technology is scaled beyond 65nm to have reduced leakage currents and remove short channel effect FinFET is most suitable device structure compared to other devices [21]. Optimization of FinFET is required for better stability and reduced power supply. This can be achieved by varying the supply, H_{fin} and also varying the threshold voltages. However, reducing the supply voltage (V_{DD}) below parametric variations can affect the cell stability. The FinFET devices are having low power dissipation .FinFET based SRAM cells provide the required power stability and also addresses the power consumption and operating voltage problems associated with devices using MOSFETs [22]. Here a 18nm FinFET technology is used to address the problems associated with power and also area up to some extent.

In nano-scale technology, power consumption is the major problem, increasing with technology node [22,23]. One possible option for reducing power consumption in a digital chip is to reduce it in static random access memories (SRAMs) because they cover a huge portion of the digital chip. This goal can be achieved by operating SRAM in a sub-threshold voltage (Vth) region, where the operating voltage is lower than the nominal voltage (VDD). However, the major drawback of the sub-Vth region is poor read stability and this leads to a considerable expansion in read static noise margin (RSNM), as a criterion of read stability, which might lead to an increase in the read failure rate [22]. Owing to less power consumption, sub-Vth SRAMs are particularly common. However, due to low VDD, they increase the probability of failure and are more sensitive to process variations. Scaling the technology node to the deep submicron and nanoscale has increased short-channel effects (SCEs) and enhanced process variations [24]. The strength ratios (channel width to channel length ratio (W/L)) and Vth of transistors are important for an SRAM cell's stability and performance, and therefore, designing a low-power SRAM cell with improved stability is very challenging. As a result, new technology has been developed to mitigate the process variations and to reduce SCEs on SRAM cell's performance. The fin-shaped field-effect transistor (FinFET) is a promising technology that can replace conventional metal–oxide semiconductor field-effect transistors (MOSFET) [25]. In integrated circuits, FinFET is adopted instead of planar CMOS. FinFETs were preferred because of their excellent properties of low leakage power, low switching voltage, high drain current, better gate control, mitigation of the SCEs with sub-Vth operation, and low retention voltages for SRAM. Offering the benefits of this technology for memory cell design, the conventional 6 T cell does not have a satisfactory performance in read and write operations at low VDD due to inconsistencies in the read and write requirements of the 6 T cell, which results in a trade-off in the transistors sizing. Exponential dependence of the sub-threshold current to the Vth of the transistors and the width quantization characteristic of FinFET exacerbates this problem [26]. Therefore, despite of device-level techniques, there is the need for development of circuit-level techniques to overcome the challenges and problems related to the 6 T SRAM cell. The common approaches presented in the literature are: Schmitt Trigger-based SRAM design , Stacking of transistors, Read-decoupling, Word line boosting , Negative bit line, Floating virtual ground (VGND) , Power-gating, Feedback-cutting, Single-ended/Single-bit line structures, Multi-Vth devices , and Bit-Interleaving (BI) architecture.

III. PROPOSED SRAM CELL DESIGN

A. Design of CMOS 6T SRAM Cell

The six-transistor CMOS SRAM depicted in figure 4. When the word lines are reduced, there is an isolation between the bit line and the access transistors [2, 8]. The high energy consumption of static SRAM is caused by the increased

leakage current. The six-transistor CMOS SRAM depicted in figure 4 has storage nodes made up of four transistors and two cross-coupled inverters.

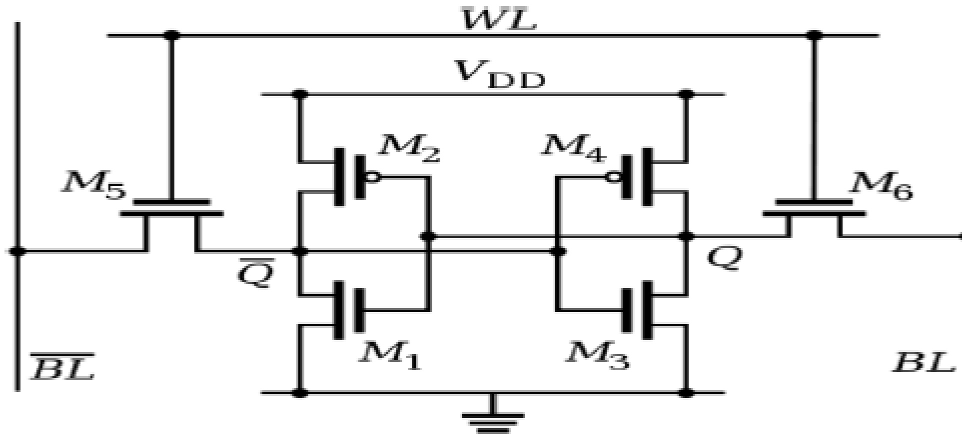


Figure 4: CMOS based 6T SRAM cell

M5, M6 transistors are utilised to access the data contained within the SRAM cell during reading and writing operations. The transistors M5 and M6 can read data from the bit lines and store it in the SRAM cell by turning on the word lines. A read-upset issue may have an impact on cell values. Between M6 and M3, a suitable transistor size is necessary to prevent QB's node voltage from falling below Vth. The pull-down transistor M3 must be more powerful since the access transistor M6 is less powerful. If this one is preserved, the data saved inside the cell will remain unchanged. In the classic CMOS architecture, the transistor ratio M3:M6 must be greater than 1.28. The BL's reading steadiness makes it unsuitable for driving Q high through M5. As a result, M6 drags node QB to the bottom and writes 0 to QB. Its access transistor M6 is more powerful than pull-up transistor M4 because pull-up transistor M4 opposes this operation. Then, as QB decreases, M1 turns off and M2 turns on, raising Q. Hence, for a better write operation, the ratio of transistors M2/M5 or M4/M6 must be lower than 1 and not higher than 1.6. This control is hence referred to as writing ability. Table 1 displays the CMOS 6 T cell size ratios at various technological nodes. The Static Noise Margin determines the stability of an SRAM cell (SNM). The cell ratios and pull-up ratios have an impact on the SRAM cell's performance as well [6] as shown in table 1. The cell ratio and pull up ratio shown in determines the read ability and write ability of the SRAM cell respectively.

Table 1 Sizing of 6T CMOS SRAM cell

Transistor width	16nm	20nm	22nm
L (M1,M,M3,M4,M5,M6)	16nm	20nm	22nm
W (M1)	32nm	40nm	42nm
W (M2)	18nm	20nm	22nm
W (M3)	32nm	40nm	42nm
W (M4)	18nm	20nm	22nm
W (M5)	16nm	22nm	26nm
W (M6)	20nm	36nm	26nm
Supply voltage (V)	0.9	0.9	0.95

B. Design of FinFET based 6T SRAM cell

FinFET technology is used to overcome the SCEs for the realization of the cell, and it is convenient to downsize underneath sub 32 nm nodes. This paper depicts the use of a double-gate (DG) FinFET 6 T cell, compared with a conventional CMOS 6 T cell. It has a significant improvement in leakage power consumption, and it examines the 6 T cell design using SG Double Gate or Tied-Gate FinFET with parameters of Fin height (Hfin), gate length (Lg), and Fin thickness (Tsi), which are tabulated in table 2.

Table 2 Transistor ratio of FinFET 6T SRAM cell

Transistors	Number of fins
Pull-up (M2,M4)	1
Pull-down (M1,M3)	3
Access transistors (M5,M6)	2

The circuit used for the FinFET 6 T cell is equivalent to the CMOS 6 T cell represented in Fig.5. except that the gate structure used here is non-planar. The number of fins selected for pull-up, pull-down, and gate transistors is shown in Table 3.2 "Under a given contact size, the maximum number of fins (Nfin) is determined by the fin thickness (Tfin) and the fin-to-fin spacing". "A fin thickness of 10-20 nm is the typical range for implementing strong electrostatic control in the double-gate scheme to reduce SCEs".

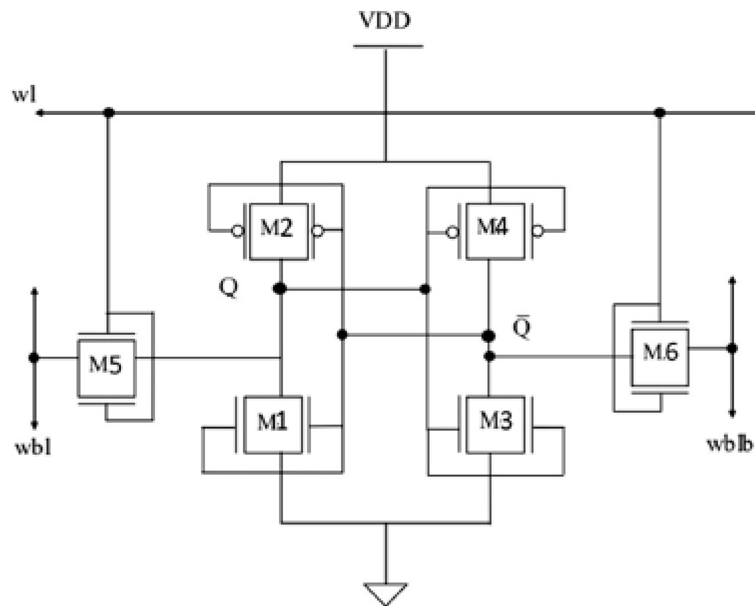


Figure 5: FinFET based 6T SRAM cell

The different operations that are supported by an SRAM cell are hold, write and read.

Hold State: In this state, the previous data in SRAM cell remains on ‘HOLD’ For Hold Operation, word line wl =0, which makes the MOS transistors M5 and M6 ‘OFF’. This isolates the SRAM cell (M1,M2,M3 and M4) from the bitlines.

Write State: In this state, the data applied at bit lines ‘wbl’ is stored in to SRAM cell. For Write Operation, word line wl =1, which makes the MOS transistors M5 and M6 ‘ON’. This makes the SRAM cell (M1,M2,M3 and M4) to accept data from the bitlines.

Read State: In this state, the data present at SRAM cell (Qor $\bar{Q}$) is sent to bit lines ‘wbl’ For Read Operation, word line wl =1, which makes the MOS transistors M5 and M6 ‘ON’.

C. **MTCMOS (Multi Threshold CMOS) Method**

SRAM cell with low threshold voltages operate faster but have higher leakage currents. On the other hand, SRAM cell with high threshold voltages have less leakage currents but suffers with more delay(slow).This technique uses two different threshold voltages in the circuit. The SRAM cell is designed using low VT transistors whereas high VT transistors are used to effectively isolate the low VT cell to prevent leakage dissipation in standby mode. Hence multi threshold logic is employed in MTCMOS method, where SRAM cell operates with low threshold voltage and power supply of SRAM are controlled through high threshold MOS transistors. Between the logic circuit and the power lines are PMOS and NMOS transistors with high VT. For real-time logical functioning, the sleep signal is activated while the system is in an active state. Transistors with higher VT values are switched off to separate the logical circuit from the power lines while it is in sleep mode. This reduces leakage current in sleep mode.

The general structure of MTCMOS is shown in figure 6 and the circuit diagram of 6T SRAM cell with MTCMOS arrangement is shown in figure 7. In active mode, high V_T transistors are turned on and low V_T SRAM cell operates such that it has low switching power dissipation and small propagation delay. During standby mode the high V_T transistors (also called as sleep transistors) are turned off and the conduction path for any sub-threshold leakage currents that may originate from low V_T cell is effectively cut off. In this configuration, leakage power dissipation is reduced for the cell; however, two extra transistors increase the area and complexity of the circuit.

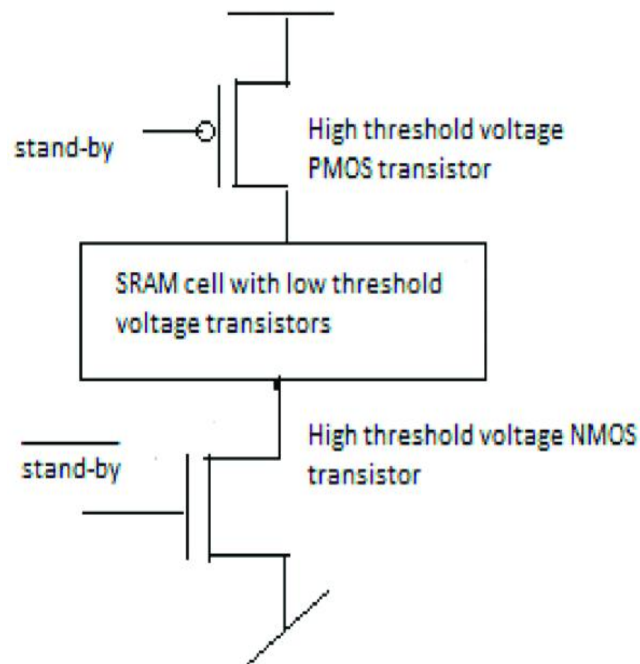


Figure 6: General structure of MTCMOS technique

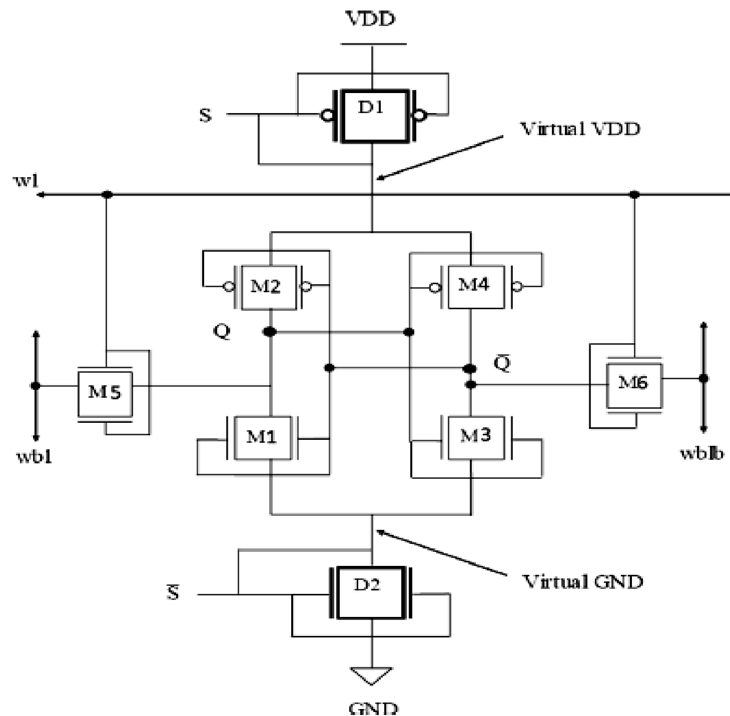


Figure 7: FinFET based 6T SRAM cell using MTCMOS technique

3.3 SVL Method (Self controllable Voltage Level)

Between V_{DD} and a 6 T FinFET SRAM cell, there is a connection made with two NMOS transistors connected in series and one PMOS transistor connected in parallel. Another circuit consisting of two series PMOS transistors connected in parallel with an NMOS transistor is connected in between the 6 T FinFET SRAM cell and GND. The circuit diagram of 6T SRAM cell with SVL arrangement is shown in figure 8.

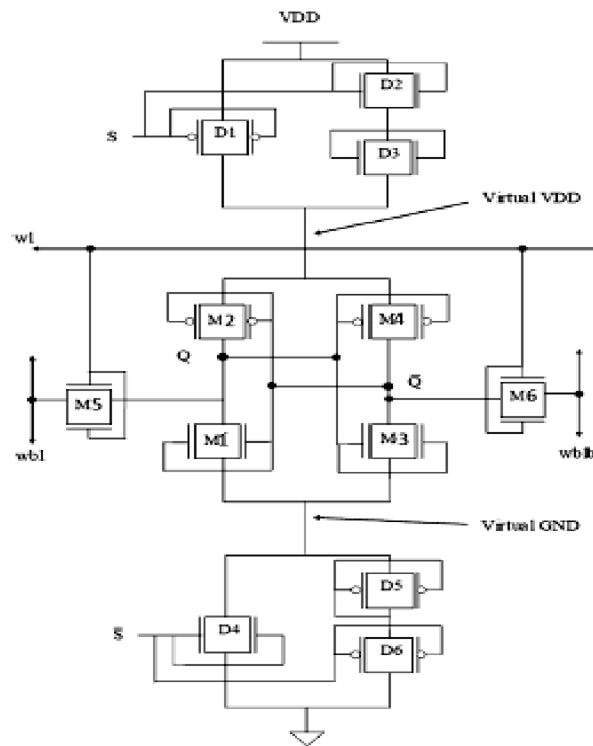


Figure 8: FinFET based 6T SRAM cell using SVL technique

Upper SVL: PMOS acts as switch and NMOS transistors acts as resistors.
In active mode, PMOS is 'ON' and connects VDD to SRAM cell while NMOS resistive network is 'OFF'. In stand-by mode, PMOS is 'OFF' and disconnects V_{DD} to SRAM cell while NMOS resistive network is 'ON'. The SRAM receives V_{DD} via multiple weak NMOS resistors, and the result is provided as follows:

$$V_P = V_{DD} - V_N \quad (3)$$

Here VN provides voltage reduction of ON N-MOS resistors. The VDSN voltage of pull-down network is provided by Eq. (3).This lowers the amount of supply applied to SRAM cell, which decreases the leakage current.
Lower SVL: NMOS acts as switch and PMOS transistors acts as resistors.
In active mode, NMOS is 'ON' and connects 'GND' to SRAM cell while PMOS resistive network is 'OFF'. In stand-by mode, NMOS is 'OFF' and disconnects 'GND' to SRAM cell while PMOS resistive network is 'ON'. This increases the amount of supply applied to SRAM cell through ground, which decreases the leakage current.

D. AVL (Adaptive Voltage Level) Method

The word adaptive refers to the fact that it adjusts its voltage dynamically in response to the demand. Due to this leakage current can be lowered and thus leakage power also can be reduced. An extra regulation circuit is utilized at the top of the circuit in the adaptive voltage level of supply (AVLS) approach to lower the supply voltage. The adaptive voltage level at ground (AVLG) approach employs a regulation circuit at the circuit's lower end to raise the ground potential. An AVL control circuit can be used either at upper side of the cell to reduce the VDD or at lower side of the cell to increase the 'GND' potential. In this technique, the supply voltage of SRAM is adjusted adaptively based on the operating state of SRAM, thereby decreasing the leakage power. The circuit diagram of 6T SRAM cell with AVL arrangement is shown in figure 9. A merger of 1 N-MOS and 2 P-MOS circuits are coupled in parallel in the AVLG approach. The N-MOS in the AVLG circuit receives an input clock pulse, and every P-MOS is linked to ground. By eliminating ground, this circuit is attached to the ground terminal of the traditional one. This could raise the circuit's ground voltage, lowering the power consumption of the traditional SRAM. In AVLS approach, a collection of 2-N-MOS and 1-P-MOS are attached in parallel.

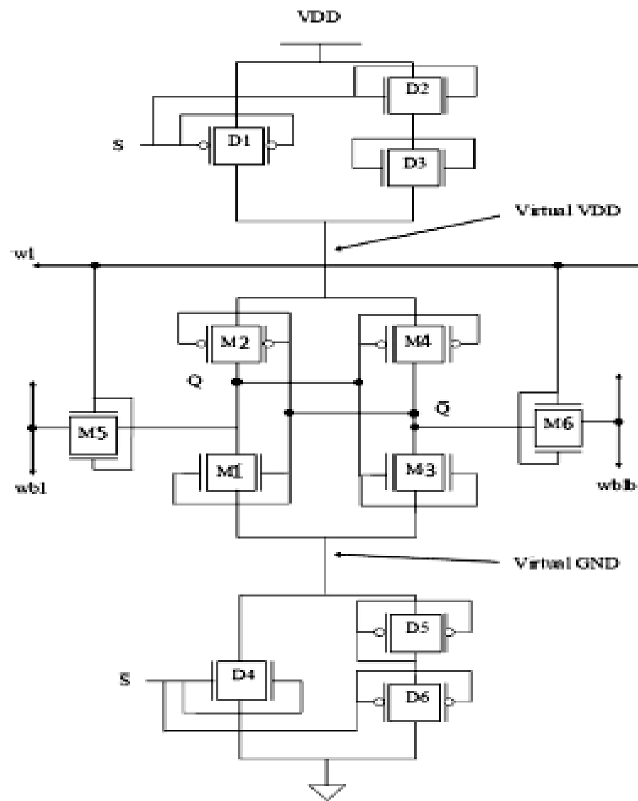


Figure 9: FinFET based 6T SRAM cell using AVL technique

Hence, an input clock pulse is employed at the P-MOS of the AVLS circuit and the remaining NMOS transistors are attached to the drain terminals. This technique is more efficient for minimizing energy utilization and for the leakage currents. This regulation circuit is located at the voltage supply source terminal of the SRAM structure where supply is provided through this regulation circuit. This regulation circuit at the top end may reduce the supply voltage provided to the entire circuit to minimize the energy utilization of the SRAM. It may minimize the leakage current by decreasing the gate to source voltage and the gate to drain voltage. This structure is useful for very low power utilization.

IV. RESULTS AND DISCUSSION

The 6T FinFET and proposed Multi threshold CMOS, SVL methods, AVL method have been simulated using Microwind EDA tool in 32 nm technology. The schematic diagram of 6T SRAM is shown in figure 10. The operation of 6T SRAM is analyzed with help of timing diagram as shown in figure 11. From the diagram, it is clear that between 2 to 4ns, the word line WL is active and hence the value applied at bit line BL is reflected at output node Q. From 4 to 6ns, the word line WL is inactive and hence the value applied at bit line BL is not reflected at output node Q, which maintains it previous value (Hold state). From 6 to 8ns, the word line WL is active again and hence the value applied at bit line BL is reflected at output node Q.

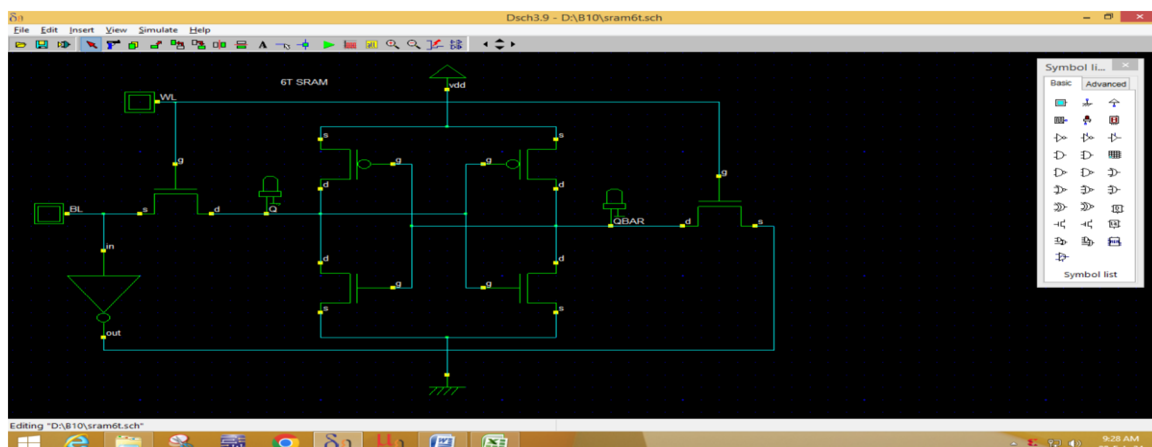


Figure 10: Schematic diagram of 6T SRAM

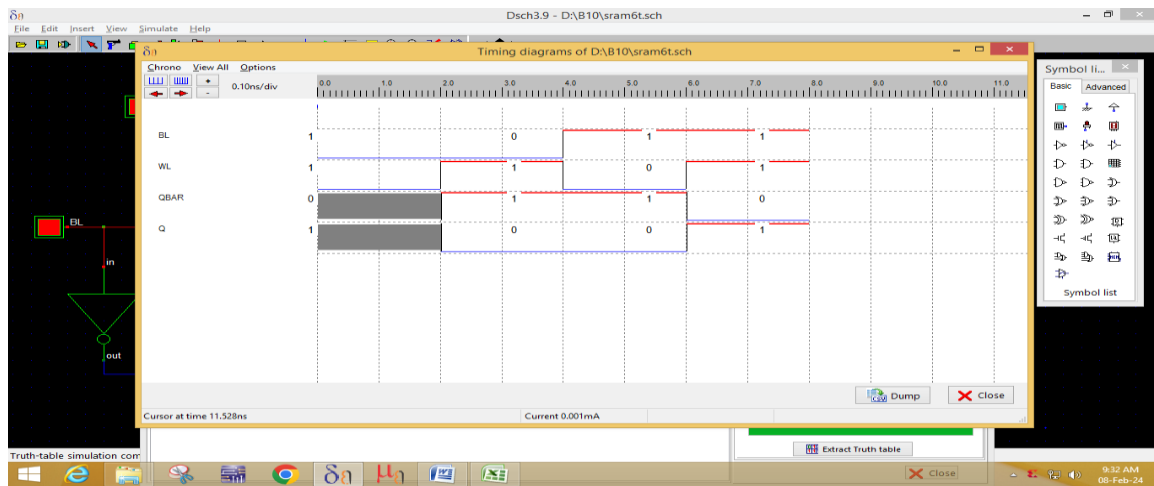


Figure 11: Timing diagram of 6T SRAM

The schematic diagram of 6T SRAM using MTCMOS is shown in figure 12. A sleep transistor of P-type is connected between V_{DD} and SRAM cell while a sleep transistor of N-type is connected between SRAM cell and ground. The operation of 6T MTCMOS SRAM is analyzed with help of timing diagram as shown in figure 13. From the diagram, it is clear that between 2 to 4ns, the sleep signal is at logic '0' , which makes sleep transistors 'ON' and connects the power supply to the circuit. Since the word line WL is active, the value applied at bit line BL is reflected at output node Q. From 4 to 8ns, the sleep signal is at logic '1' , which makes sleep transistors 'OFF' and disconnects the power supply to the circuit and the cell maintains its previous value at output node Q (Hold state).

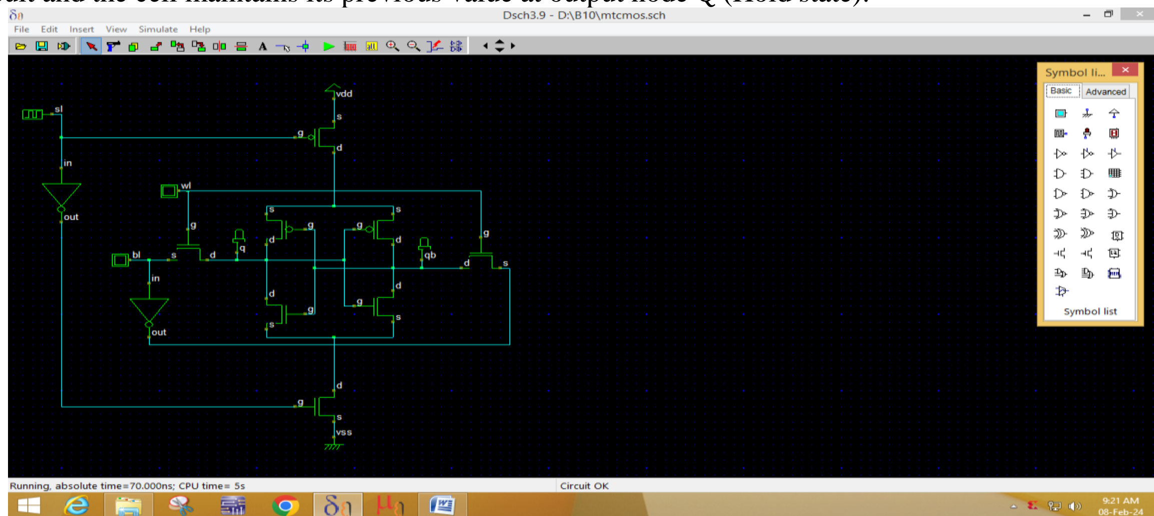


Figure 12: schematic diagram of 6T SRAM using MTCMOS

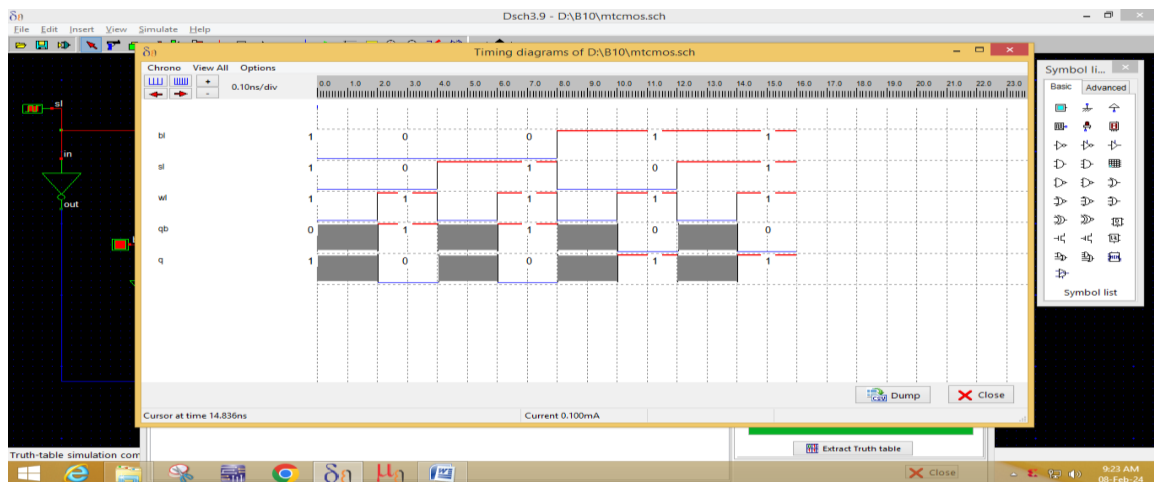


Figure 13: Timing diagram of 6T SRAM using MTCMOS

The schematic diagram of 6T SRAM using SVL is shown in figure 14. A switch of P-type and resistors of N-type are connected between V_{DD} and SRAM cell while a switch of N-type and resistors of P-type connected between SRAM cell and ground.

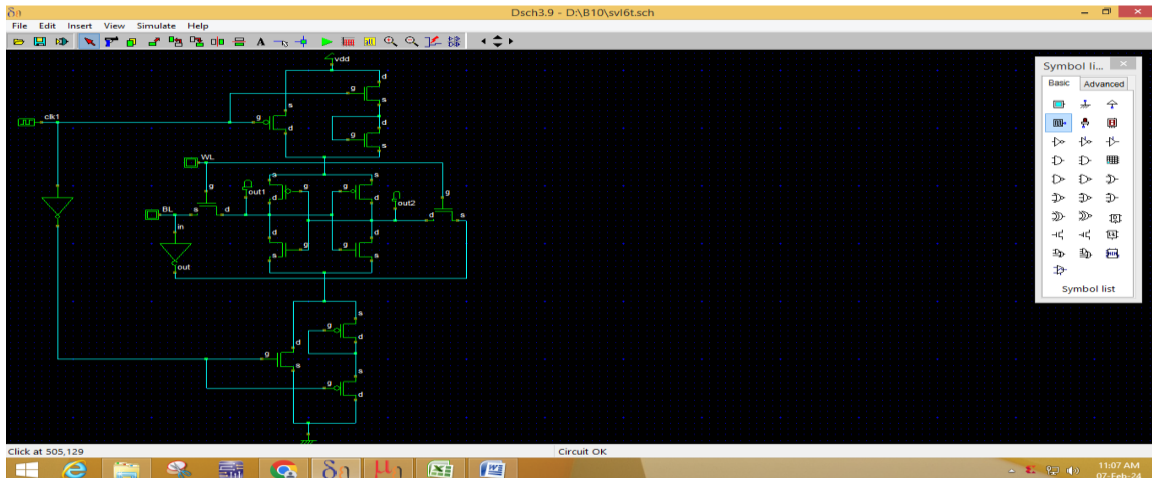


Figure 14: schematic diagram of 6T SRAM using SVL

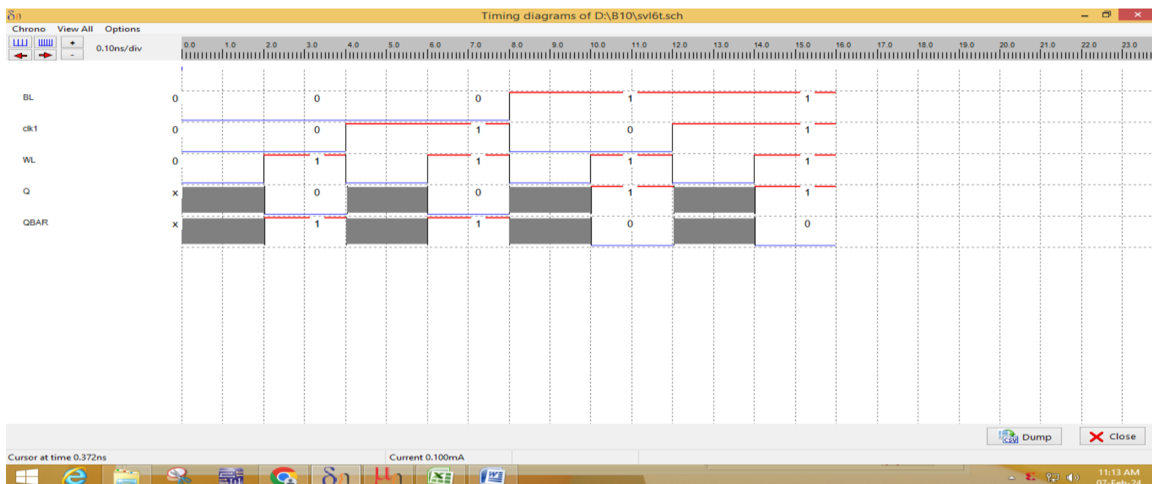


Figure 15: Timing diagram of 6T SRAM using SVL

The operation of 6T SVL SRAM is analyzed with help of timing diagram as shown in figure 15. From the diagram, it is clear that between 2 to 4ns, the clock signal is at logic '0' , which makes D1 and D4 transistors 'ON' and connects the power supply to the circuit. Since the word line WL is active, the value applied at bit line BL is reflected at output node Q. From 4 to 8ns, the clock signal is at logic '1' , which makes D1 and D4 transistors 'OFF' and connects the power supply to the circuit through D2,D3, D5 and D6 resistive transistors and the cell maintains its previous value at output node Q (Hold state).

Implementation AVL would be similar to SVL, but instead of diminishing the ability of virtual VDD, the potential of virtual ground should be adaptively increased. The word adaptive refers to the fact that it adjusts its voltage dynamically in response to the demand. Due to this leakage current can be lowered and thus leakage power also can be reduced. An extra regulation circuit is utilized at the top of the circuit in the adaptive voltage level of supply (AVLS) approach to lower the supply voltage. The adaptive voltage level at ground (AVLG) approach employs a regulation circuit at the circuit's lower end to raise the ground potential.

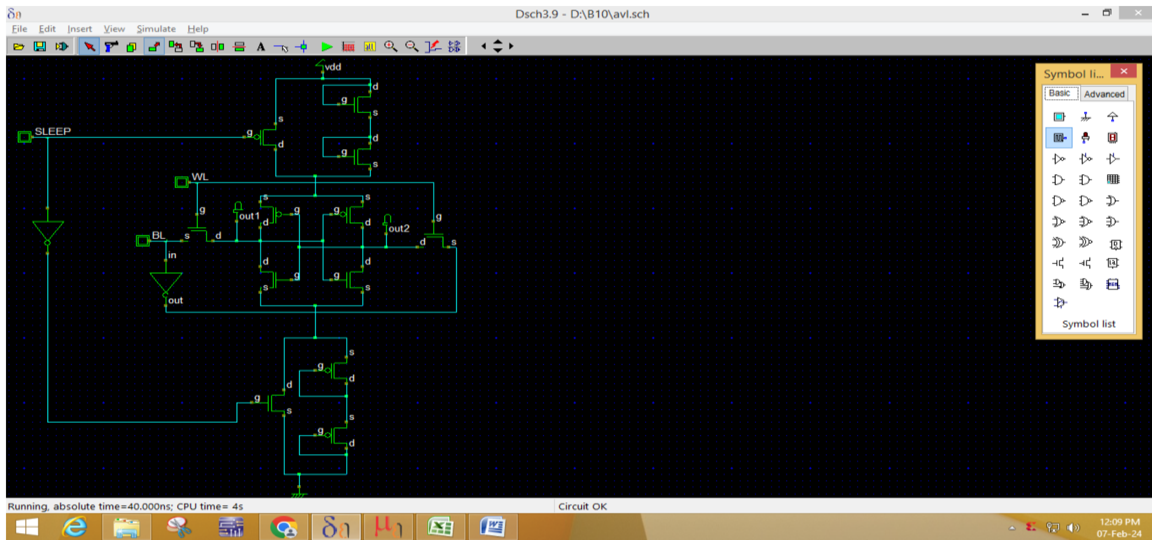


Figure 16: Schematic diagram of 6T SRAM using AVL

A comparative analysis is made in terms of delay and power dissipation between conventional 6T SRAM and 6T SRAM cell employing MTCMOS, AVL and SVL techniques for various power supply voltages. The power dissipation of 6T SRAM cell along with rise time, fall time and delay is presented in table 3 for supply voltage varying from 0 to 2.5V with an incremental value of 0.5V. The power dissipation of 6T SRAM cell employing leakage power reduction techniques along with rise time, fall time and delay is presented from tables 4 to 6 for MTCMOS, AVL and SVL respectively.

Table 3 Delay and power dissipation of 6T SRAM at various V_{DD}

V_{DD}(V)	t_r (ps)	t_f (ps)	Delay (ps)	Power dissipation(mW)
0	0.000	0.000	0.000	0.000
0.5	0.000	0.000	0.000	0.002
1	0.000	0.000	0.000	0.009
1.5	79.500	0.000	39.750	0.033
2	30.900	17.700	22.650	0.150
2.5	14.300	11.500	12.990	0.259

Table 4 Delay and power dissipation of 6T MTCMOS SRAM at various V_{DD}

V_{DD}(V)	t_r (ps)	t_f (ps)	Delay (ps)	Power dissipation(mW)
0	0.000	0.000	0.000	0.000
0.5	16.200	50.150	33.100	0.002
1	67.750	4.050	35.870	0.009
1.5	43.600	5.950	24.500	0.027
2	36.150	7.550	21.820	0.050
2.5	30.100	9.250	19.620	0.091

Table 5 Delay and power dissipation of 6T AVL SRAM at various V_{DD}

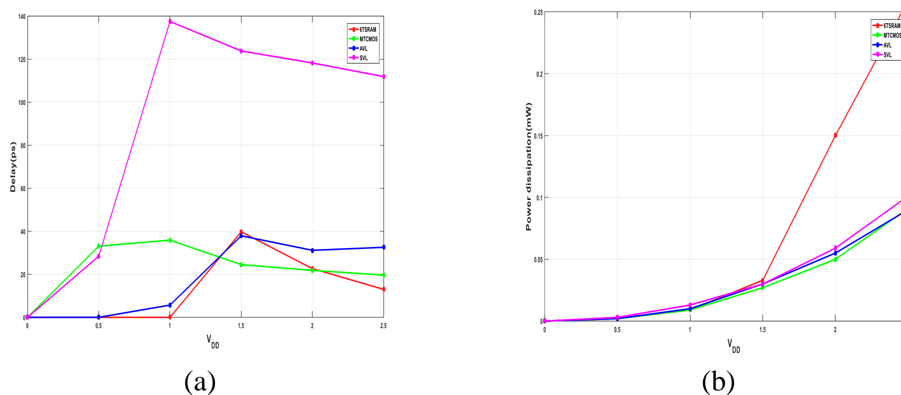
V_{DD}(V)	t_r (ps)	t_f (ps)	Delay (ps)	Power dissipation(mW)
0	0.000	0.000	0.000	0.000
0.5	56.900	0.000	0.000	0.002

V_{DD}(V)	t_r (ps)	t_f (ps)	Delay (ps)	Power dissipation(mW)
1	172.500	103.300	5.700	0.010
1.5	143.900	104.700	37.900	0.030
2	130.300	106.300	31.150	0.055
2.5	117.000	106.900	32.550	0.090

Table 6 Delay and power dissipation of 6T SVL SRAM at various V_{DD}

V_{DD}(V)	t_r (ps)	t_f (ps)	Delay (ps)	Power dissipation(mW)
0	0.000	0.000	0.000	0.000
0.5	0.000	0.000	28.400	0.003
1	11.450	0.000	137.500	0.013
1.5	75.850	0.000	123.800	0.030
2	59.700	2.600	118.200	0.059
2.5	46.850	25.000	111.880	0.101

Analysis of delay in picoseconds reveal that from V_{DD} = 0 to 0.5V, 6T SRAM and SRAM with AVL offered less delay compared to SRAM with MTCMOS and SVL. From V_{DD} = 0.5V to 1.5V, delay of 6T SRAM and SRAM with AVL increased linearly while delay generated by MTCMOS and SVL started decreasing with MTCMOS providing less delay among all techniques at V_{DD} = 1.5V. At V_{DD} = 2V, delay generated from 6T SRAM and MTCMOS are same and at V_{DD} = 2.5V, compared to all leakage reduction techniques, 6T SRAM provided less delay as shown in figure 17 (a).Analysis of power dissipation in microwatts reveal that from V_{DD} = 0 to 1.5V, 6T SRAM and SRAM with all leakage reduction methods offered same power dissipation. From V_{DD} = 1.5V, as supply voltage increases, the power dissipation of 6T SRAM increased linearly while power dissipation of same cell when operated with leakage reduction techniques, even though increased with supply voltage , it is less when compared with conventional 6T SRAM as shown in figure 17(b). Among leakage reduction techniques, MTCMOS offered less power dissipation at V_{DD} = 2V while at V_{DD} = 2.5.V, SRAM with AVL provided better performance in terms of power dissipation.



(a) (b)

Figure 17: (a) Delay analysis and (b) Power analysis of various 6T SRAM cells

V. CONCLUSION

In this paper, FinFET technology was used in the design of the 6 T SRAM, and it was found that while the FinFET-based 6 T cell has equal static power dissipation, its dynamic power dissipation is lowered by 1.6 times when compared to the CMOS-based design. That is, compared to the conventional architecture, the FinFET-based 6 T cell device uses a lot less power. It also has 26% better RSNM and 18% better hold SNM. Several techniques for minimizing leakage current were applied to a FinFET 6 T-SRAM cell. We can plainly observe a decrease in the leakage current dissipated in the SRAM cell following the application of leakage current reduction strategies as compared to the FinFET 6 T-

SRAM cell. MTCMOS and AVL offer the best leakage power reduction and the least amount of leakage current out of all the approaches discussed.

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