Substrate Level Noise Analysis Tool (SNAT) in Mixed Signal circuits

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***Abstract*: There exist several tools that can be used to predict the substrate noise profile of digital systems. However, none of these are flexible enough to work at any stage in the design cycle. These tools can only be used for final verification. Final verification of the substrate noise performance of a digital system is an important part of substrate coupling analysis. However, a tool that can yield information at earlier stages in the design cycle permits changes in both the design and the layout to try and mitigate noise coupling and, thus, performs a much more valuable function. Such a tool should be able to work at higher abstraction levels to tradeoff accuracy for simulation speed.**

1.1 Introduction.

The basic arrangement of substrate Noise Analysis tools (SNAT) shown in figure 1.1SNAT requires two inputs: a circuit description and a technology description. SNAT decomposes the circuit into equivalent noise macro models. The noise macro models together with the event model for each node in the circuit are used to construct the noise signature. This noise signature is then simulated with the substrate model and power grid to compute the substrate noise profile. The outputs are a time domain representation and noise spectrum. The details of each of these steps are the subject of this are below.

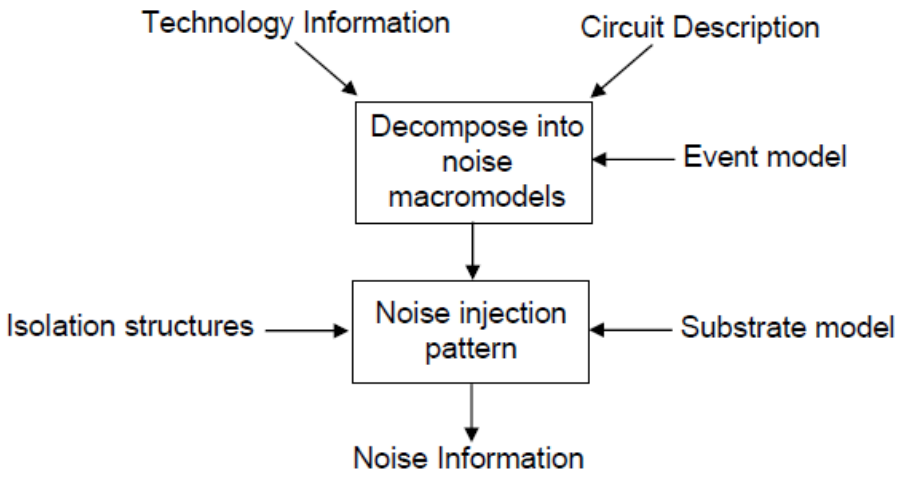

Figure 1-1: High level block diagram of SNAT.

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1.2 Granularity Level.

SNAT works with a broad spectrum of information for both the circuit and technologydescriptions. This allows SNAT to be used at any stage in the design cycle. The different input descriptions that SNAT can work with are detailed in Figure 1-2 and
Figure1-3.

1.2.1 Circuit Description.

To generate the noise signature, SNAT requires information on the circuit. At a minimum, a gate-level description along with BSIM models can be used to generate the signature. At the gate level, no layout information is available; thus, the noise sources will not be accurately modeled. Because very little information is available, the simulation time will be fast; however, accuracy will be compromised.

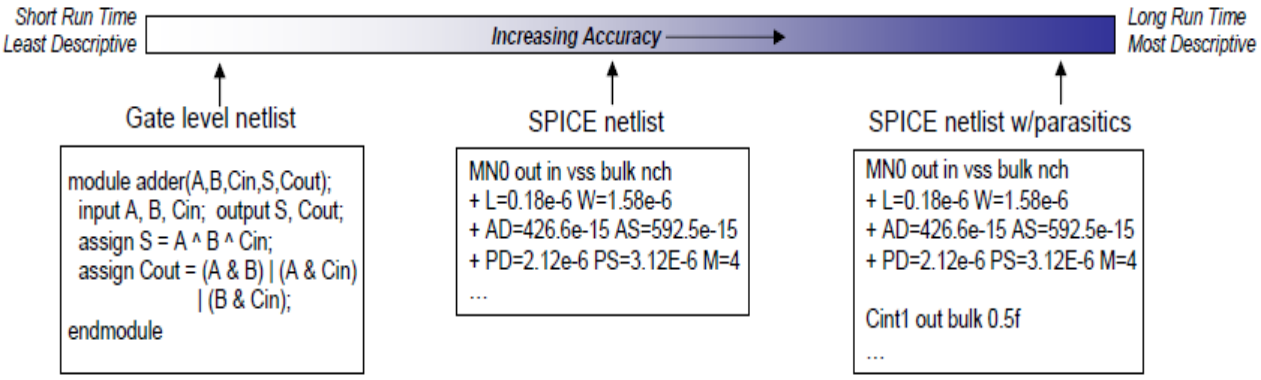

Figure 1-2: Granularity levels for the circuit description.

As the user provides more information to the tool, the noise sources will be modeled more accurately improving the overall accuracy of the simulation. However, more nodes are now considered. As a result, the simulation time increases. For instance, providing a more detailed circuit description such as an extracted netlist from layout increases the number of elements that are simulated and thus the run time; however, the accuracy increases. SNAT's ability to work with a variety of input descriptions is referred to as the granularity level.

1.2.2 Technology Description.

Multiple granularity levels are also present on the substrate modeling side. To properly model the high resistivity, non-epi substrate that is typically used in mixed-signal systems, a full extraction of the layout of the circuit with the substrate doping profile has to be generated. Cadence's SubstrateStorm tool is typically used for detailed extraction. SubstrateStorm requires both a layout and substrate doping profile.

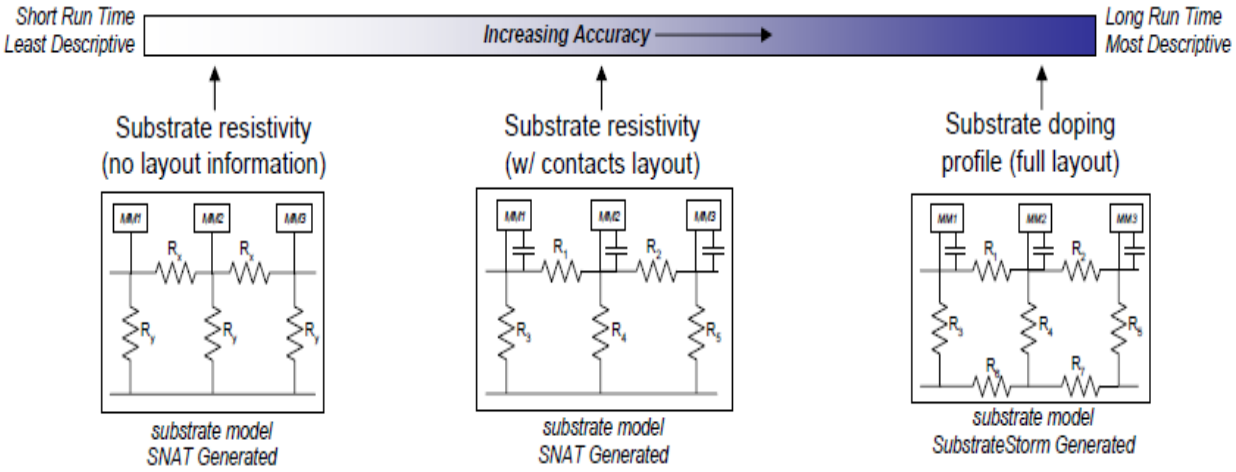

Figure 1-3: Granularity levels for the technology description.

Depending on the size of the circuit, the generated netlist can be massive since allpropagation mechanisms are accounted for. It is not unusual for the resultant netlist to consist of several million elements. Using such a complete substrate model results in the most accurate estimate at the expense of a long run time. Simulation times are on the order of several days for a medium-scale circuit. Such long run times can be tolerated for final verification; however, they are prohibitively long if the simulation is performed during the designphase.If the technology is not well characterized, substrate doping profiles might not be available. In this case, Substrate Storm cannot be used to generate a model. SNAT can work with a substrate model generated from an outside source or can generate its own substrate model.

At the next lowest granularity level, SNAT generates a coarser substrate modelknowing only the underlying substrate resistivity. It will later be shown that the capacitive effects of wells and other junctions need only be considered at lower frequencies. At higher frequencies, the resistive nature of the substrate dominates. This observation is the basis of the coarser substrate model. Based on the layout, a purely resistive model is generated. This model is a mesh of resistances between the substrate contact locations. The number of nodes is greatlyreduced speeding up run time. The user can also choose to give a less detailed layout rom which a substrate model can be generated. With the reduced detail, the number of elements in the substrate model decreases speeding up run time.

SNAT also has to be able to yield a substrate model when no layout information is available. For example, if the circuit

input description is a verilog netlist, no layout is available. SNAT can still yield an approximation for the substrate noise levels with no circuit layout. To generate the substrate model for such a case, an estimate of the circuit area must be provided from which a resistive substrate model is generated. In this case, an equi-resistance mesh is generated.

1.3Macromodel.

SNAT generates equivalent macromodels for each gate. The macromodel used is a modification of that proposed in. Figure 1-4 shows all the noise sources in a digital system. In order to accurately model noise injection, all noise sources must be accounted for. Each element in the macromodel is used to model a noise source. Figure 1-5 shows the SNAT macromodel.

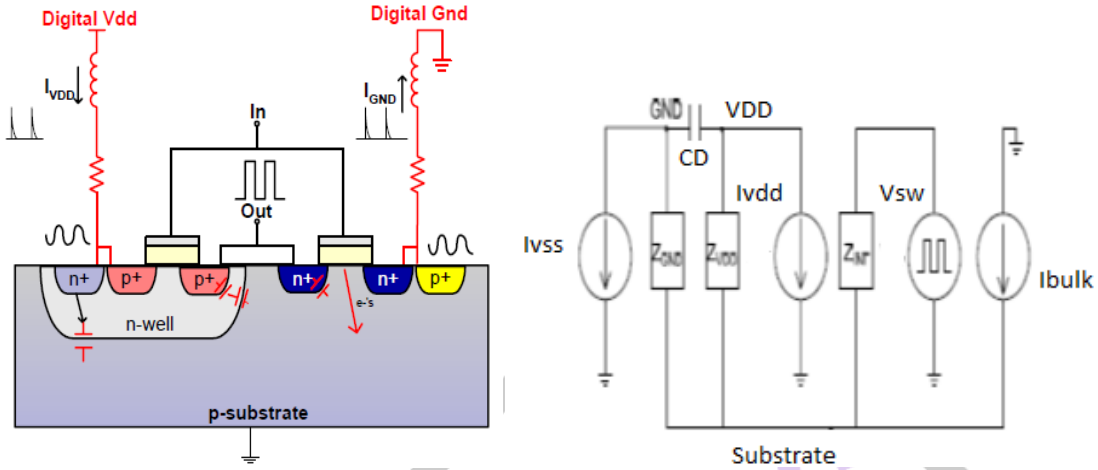

Figure 1-4: Substrate noise sources in a digital system.Figure 1-5: SNAT noise macromodel

The current sources I_{VDD} and I_{VSS} represent the noise in the power and ground lines respectively. These currents working in tandem with package parasitics will create V_{DD} and ground bounce that appears on the substrate. Z_{GND} and Z_{VDD} represent the equivalent impedance from ground and V_{DD} respectively to substrate. For example, for a simple n-well process, Z_{GND} could simply be the resistance of the substrate contact, Rsub. Z_{VDD} would be the series combination of the n-well capacitor and the resistance through the n-well. C_D represents the impedance local to the gate betweenV_{DD} and ground.Modeling the impedance from the both V_{DD} and ground to substrate as simplelumped elements is an approximation that is valid up to several GHz.IMEC comparedthis model to a more accurate model generated by LAYIN (now SubstrateStorm) for an inverter.

The lumped model in the macromodel loses its validity around 5 GHzfor an inverterhundred switching transistors. However, the complex routing of the interconnect mesh does create a shielding effect that mitigates the amount of noise that is coupled.Nevertheless, in some situations certain interconnect can induce significant levels of substrate noise. For example, interconnect associated with clock networks is used to distribute a high-speed signal using wide metal traces that can have significant capacitance to substrate. Other approaches neglect this source of noise resulting in reduced accuracy when compared to measured data. The current noise sources in the macromodel depend on both the input rise time and output load.

1.3.1 Rise Time Dependency

Figure 1-6 shows how the current profile changes with input rise time for an inverter designed in a 0.18 µm technology. With increasing rise time, the peak reduces while the pulse width widens. To accurately re-create the current pulses, the rise time of the inputs of each gatemust be determined. This is obtained from an event-driven simulation of the digitalcircuit.

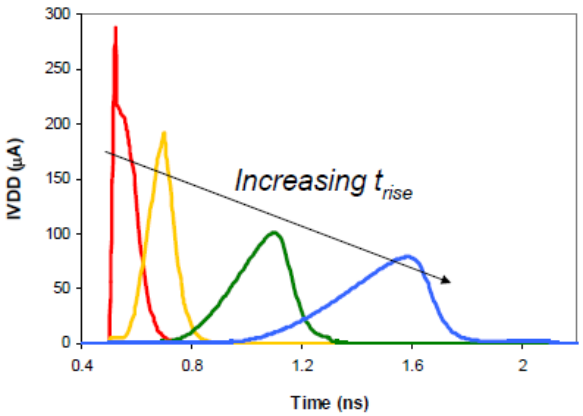

Figure 1-6: Macromodel noise current dependence on input rise time.

1.3.2 Output Load Dependency

The pulse shape of the noise current sources also depends on the output load if an output switching event occurs. For an inverter, Figure 1-7 shows that up to a particular load level, the peak increases; however, after a certain point, the peak remains constant. The fall time of the current transient increases with increasing load.

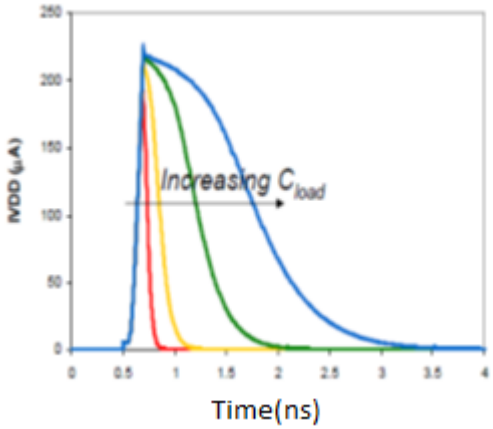

Figure 1-7: Macromodel noise current dependence on the output load.

In order to accurately re-create the current pulse, the load at each node of thecircuit must be determined. The dependency on both the input rise time and output load is specific to each cell and is extracted during the library characterization step. This step need only be performed once per technology library and takes approximately 18 hours to characterize 471 standard cells on a dual processor 1.2 GHz SunFire 280r machine.

1.4 Methodology.

Figure 1-8 outlines the methodology used by SNAT. The first step in the methodology is to characterize all the cells in the library. The dependencies on input rise time and output load are extracted and stored during this library characterization. The dependencies are unique to each cell. For example, the function describing the peak dependence of IV_{DD} on input rise time for an inverter will differ from that of a NAND gate. In addition, the impedance elements in the macromodel are extracted throughan AC SPICE simulation for each gate.

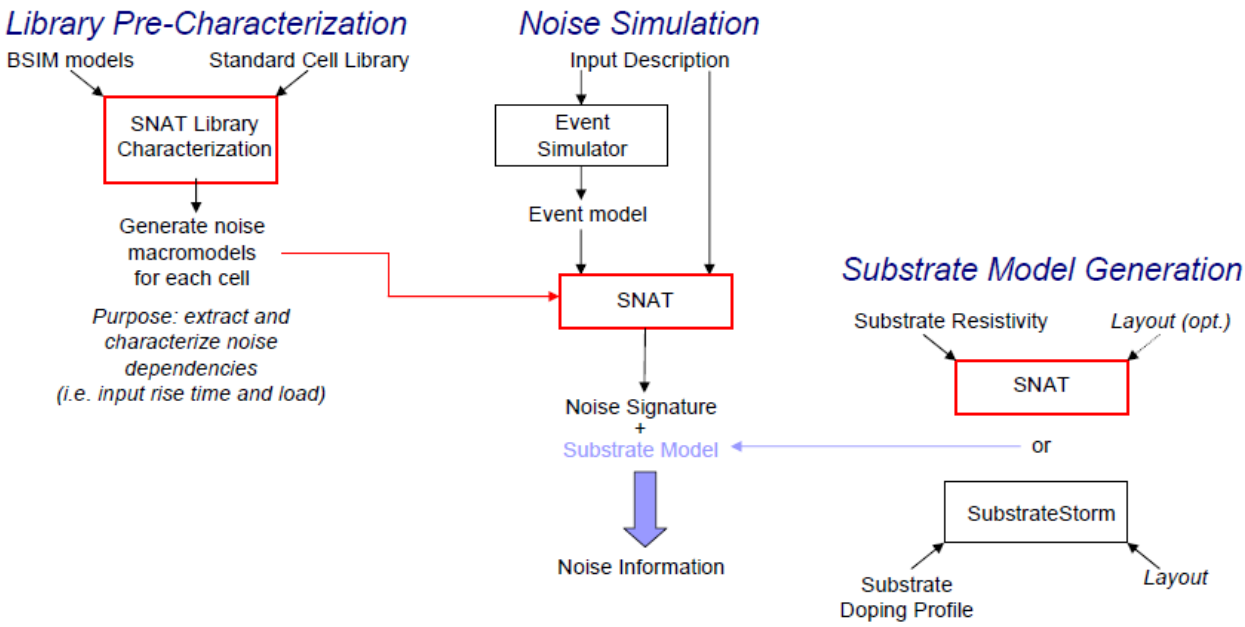

Figure 1-8: SNAT methodology.

This library characterization step takes approximately 18 hours to characterizeTSMC's 0.18 µm standard cell library on a 1.2 GHz SunFire 280r machine.The characterization algorithm used is more efficient than that of SWAN. The characterization step in SWAN takes approximately 39 hours to characterize 96 standard cellson a Pentium R 2. The reason for this speed up is not clear as their algorithm has not been disclosed. The library characterization need only be performed once per technology library.The second step in the methodology is to perform the substrate noise simulation itself. In order to accurately re-create the noise waveform, the noise sources in themacromodel must be modeled accurately. The current pulses of a particular gate depend on the input rise and fall time and on the output load if an output switching event occurs. In order to generate the correct pulse, this information needs to be determined.

An event driven simulation is performed on the full system in orderto record the rise and fall times of each node and the state of all nodes at eachpoint in time. If the input description is a gate level netlist, a gate level simulation isperformed. If the input description is a SPICE netlist, Nanosim is used to generate the event model. SNAT decomposes the full circuit into equivalent macromodels. From the eventmodel, the relevant parameters are extracted to re-create the noise current pulses for each gate. The complete macromodel for each gate of the design is then constructed.The macromodels are then connected together with a substrate model. If a model for the power grid is supplied, the model is incorporated between the local powersupply nodes. The substrate model can be generated in one of two ways. The model could begenerated from an external tool such as SubstrateStorm. This model can then beinput into SNAT.

If a very accurate substrate model is required, this option must beexercised as the models generated by SNAT are less accurate. Moreover, SNAT itselfcould be used to generate the substrate model. SNAT should be used to generate themodel if a speedup in simulation is required or if the layout or technology is not welldeveloped.SNAT takes the constructed equivalent circuit that consists entirely of linear elementsand uses SPICE as the engine to compute the substrate noise profile. SNATdetermines both the time domain noise and the noise spectrum. The effect of different isolation structures on the substrate noise profile can alsobe determined. The user specifies the isolation geometry and distance, and SNATshows the resultant substrate noise profile. Currently, SNAT only works with guardring isolation.

1.5 Example.

The operation of SNAT is best understood through an example. During the librarycharacterization, SNAT characterizes each of the standard cells and generates equivalent macromodels. In order to extract the current profiles, SPICE simulations over all possible input combinations are performed, and the resultant profiles are stored. In addition, the dependencies on rise time and load are also extracted. The final elements that must be extracted are the equivalent impedances. Z_{GND}, Z_{VDD}, and Z_{int} are calculated based on the geometry of each device and on resistance and capacitance data provided in the BSIM model file. For an NMOS device in an n-well process, Z_{GND} is typically the resistance of the p+ substrate contact. For a PMOS device, Z_{VDD} consists of the series combination of the n-well capacitance and the resistance of the n+ substrate contact. Z_{int} represents the impedance from switching interconnects to the substrate and is typically a series resistance and capacitance. For example, to incorporate the effect of a switching signal connected to an output pad, Zconsists of a series capacitance representing the pad to substrate capacitance and a resistance representing a spreading resistance. CD is extracted from an AC simulation of each cell.

All this information is stored in a look-up table that is accessed during the substrate noise simulation. Figure 1-09 shows the schematic of a one bit adder. For this example, the input to the tool is a verilog netlist that describes this adder. Figure 1-10 shows the synthesized verilog netlist. SNAT identifies each of the standard cells in the design. For the one bit adder example,

those cells are AOI22X1, XOR2X1, and INVX1. It then replaces each cell with its equivalent macromodel. A gate-level simulation is performed to extract the switching events of each node of the adder. This event information together with the look-up table generated during the library pre-characterization is used to construct the noise current waveforms for each macromodel. For example, consider constructing

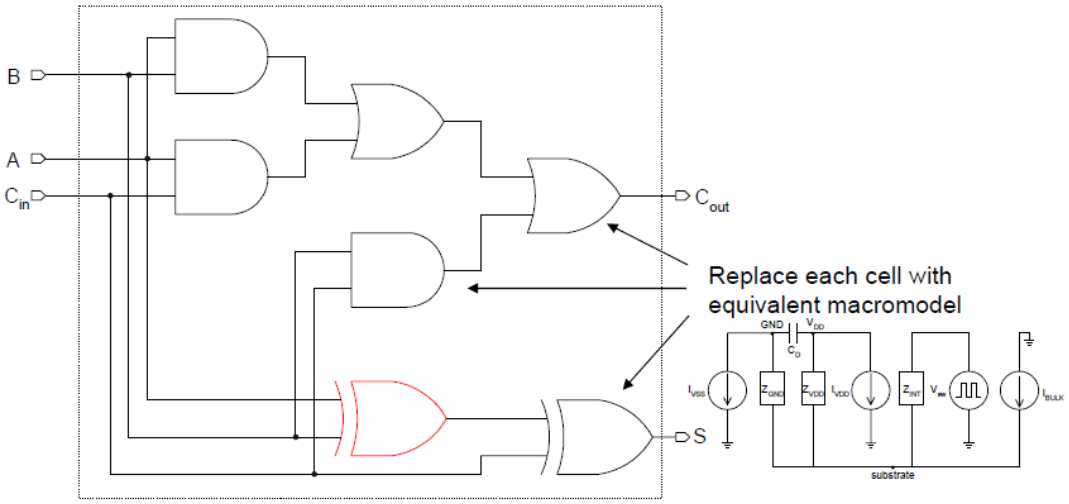

Figure 1-09: One bit adder example.

```
module adder1b ( A, B, Ci, S, Co );
input A, B, Ci;
output S, Co;
wire n4, n5;
AOI22X1 U7 ( .A0(B), .A1(A), .B0(n5), .B1(Ci), .Y(n4) );
XOR2X1 U8 ( .A(A), .B(B), .Y(n5) );
XOR2X1 U9 ( .A(Ci), .B(n5), .Y(S) );
INVX1 U10 ( .A(n4), .Y(Co) );
Endmodule
```

Figure 1-10: Synthesized verilog netlist for the one bit adder example.

the current profiles for the XOR gate highlighted in Figure 1-11. Figure 1-12 showsthe node transitions. The event information indicates that node B switches from low to high at t=0.5 ns with a rise time of 0.1 ns. Node A remains low. The output switches from low to high as a result of the transition on node A. With the information that node B transitions from low to high with a rise time of 0.1 ns while node A remains low, SNAT reconstructs the current profile using the stored current profile from the library pre-characterization. Because an output switching event occurred, SNAT calculates the output node capacitance, and reconstructs the current profile for the load. The resultant currentprofiles are shown in Figure 1-13.

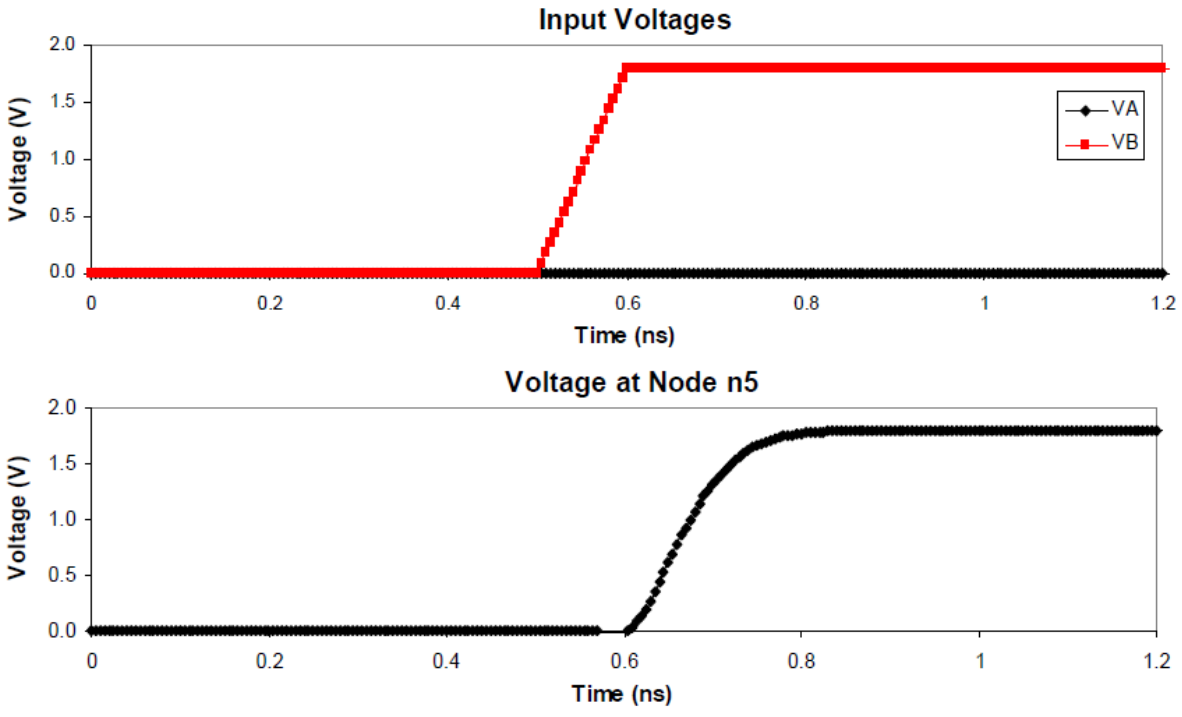

Figure 1-11: Node transitions for the XOR gate in the one bit adder example.

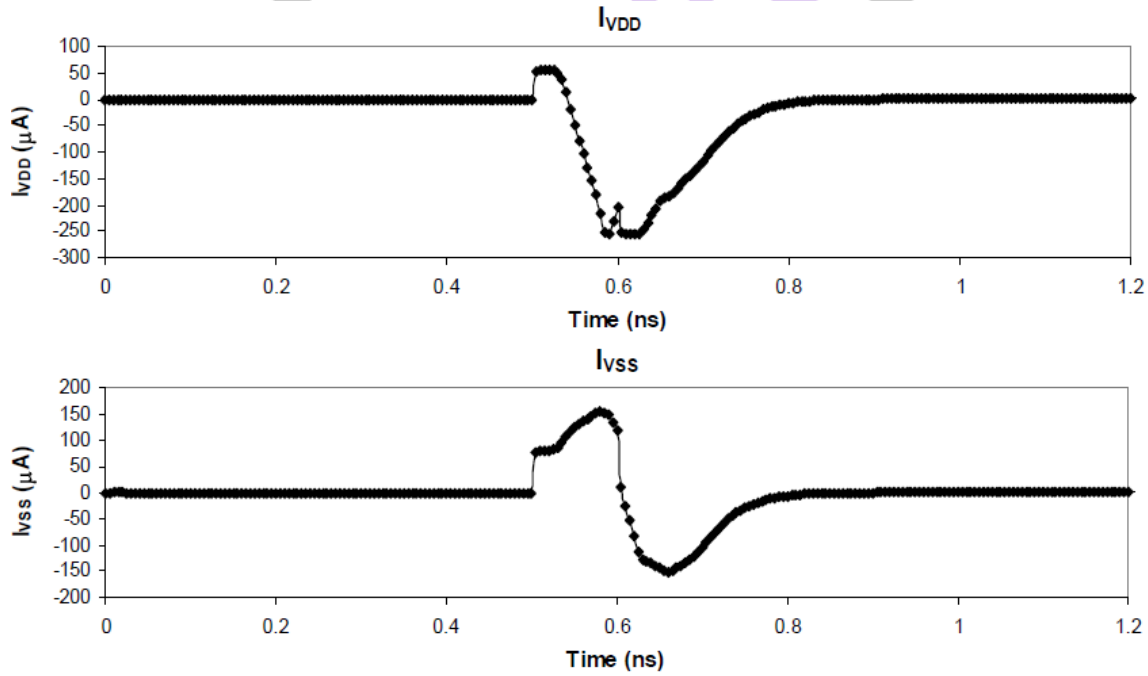

Figure 1-13: SNAT-constructed current profiles for the XOR gate in the one bit adder example.

The macromodel for the XOR gate is constructed by referring to the pre characterization library for the other element values and combining this information with the constructed current and voltage profiles. This procedure is repeated for each of the standard cells in the design. The resultant macromodels are combined together with a substrate model to form the final circuit. This is shown in Figure 1-13. Because of the small size of the circuit,a single substrate node was assumed. If a non-epi substrate is used, the macromodelsare combined with a substrate model as shown in Figure 1-14.

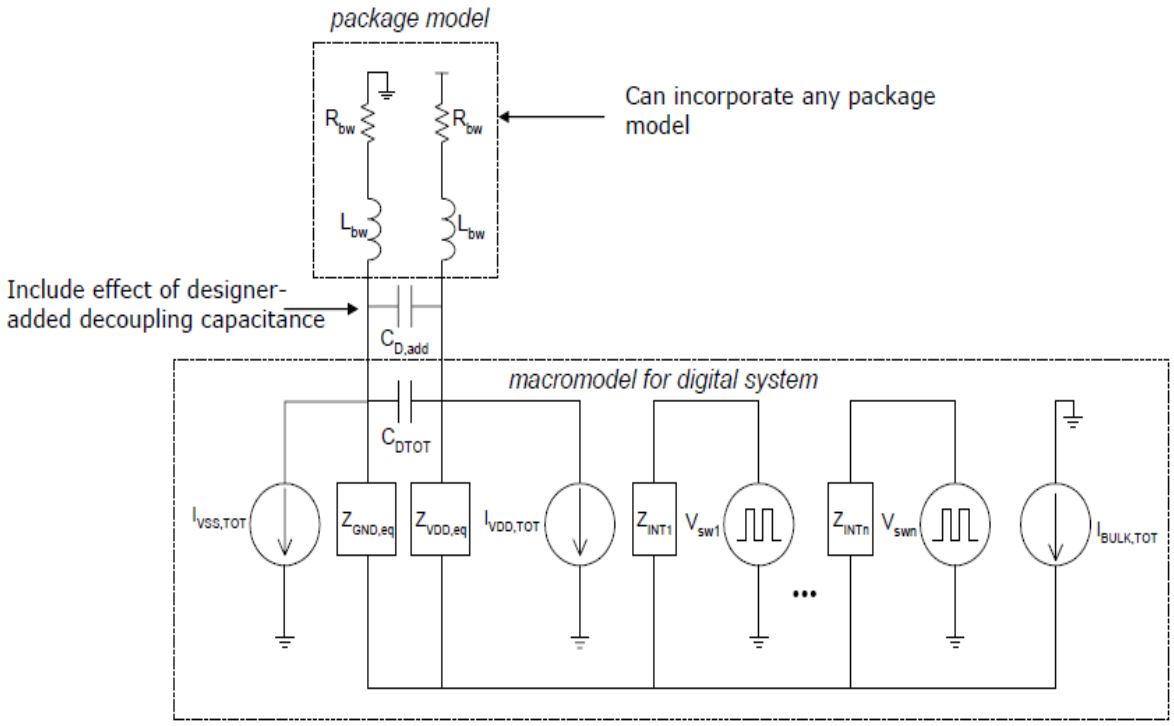

Figure 1-13: Equivalent circuit generated by SNAT for the one bit adder.

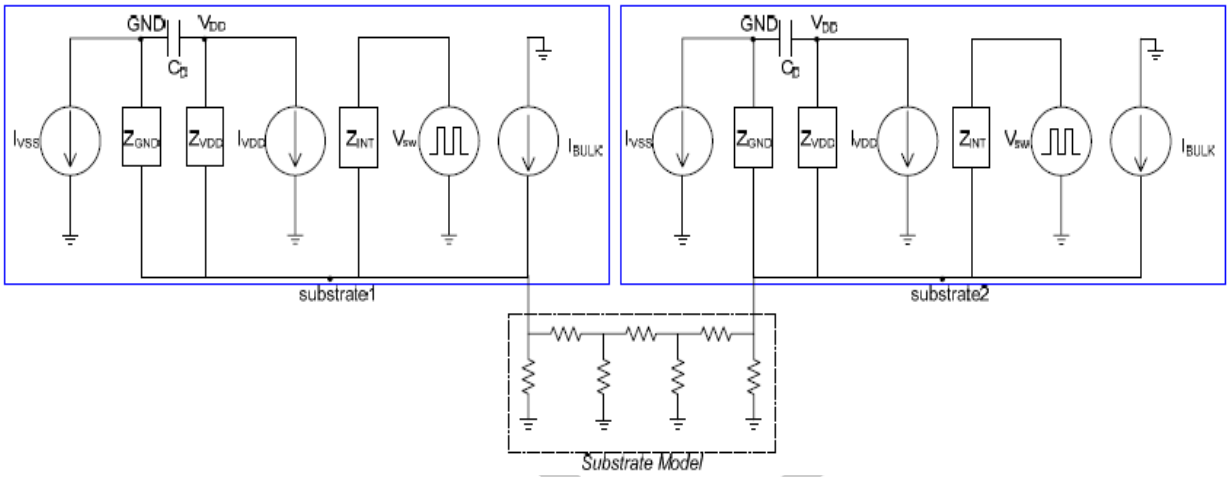

Figure 1-14: Equivalent circuit generated by SNAT for a system on a non-epi substrate.

The package plays an important role in the generated noise profile. The user must enter a package model. For this example, a simple series resistance and inductance is used to model the bondwire. The effect of user-added decoupling capacitance can also be considered. SNAT simulates this equivalent circuit to extract the substratenoise profile.

1.6 Conclusion

A CAD tool that can be used to predict substrate noise generation of any digital system at any point in the design cycle was presented. Simulation times are greatlyreduced by using a macromodel approach. Further reduction in run time can beachieved at the expense of accuracy. The tool can be used at any stage in the designcycle from preliminarily evaluating the substrate noise performance to doing a fullchip final verification.

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