Design of a Robust 13T SRAM Bitcell for Operation in Low Voltages

[1]S.Gokilapriya,[2]Dr.O.Saraniya

[1]PG Scholar, [2]Assistant Professor
Department of Electronics and Communication Engineering,
Government College of Technology, Coimbatore, India

***Abstract*—Continuous transistor scaling, coupled with growing demand for low-voltage operation, near the device threshold voltage (V_T) increases the susceptibility of VLSI circuits to soft errors, especially when exposed to high radiating environments. The most vulnerable of these circuits are memory arrays that are susceptible to radiation effects than circuits powered at nominal supply voltages. Soft errors like Single Event Upsets (SEUs) occur when an energetic particle hits a sensitive node in a circuit, a transient current pulse generated due to an injected charge, changes the node voltage causing a bit flip in the memory cell. Radiation hardening of such memory blocks is achieved by implementing large bitcells or using Error-Correcting Codes (ECCs). But ECC may entail significant area, performance, and power dissipation penalties. Also, ECC only detects and corrects the error at the time the faulty word is being read, not when it occurs. So, Radiation-Harden-By-Design (RHBD) techniques are targeted at memory cells. The proposed radiation-hardened 13T Static Random Access Memory (SRAM) targeted at low-voltage functionality maintains high soft-error robustness. It employs dual-driven separated-feedback mechanism to tolerate upsets with charge deposits of 500fC. The cell provides better immunity to soft errors when compared to 6T SRAM cell. A 4x4 memory macro was designed and tested using LFSR showing read and write functionality at a scaled voltage of 1V.**

***IndexTerms*—critical charge, low voltage, radiation hardening, single event upset (SEU), static random access memory (SRAM), linear feedback shift register (LFSR), memory array.**

I. INTRODUCTION

In the development of semiconductor technology, CMOS downscaling has brought about significant performance improvements. In the current nanoscale VLSI design, power dissipation is the one of the most important aspect. Ultra-Low Power (ULP) operation in VLSI chips particularly for space applications is of great importance where the available energy resources are limited. In future, low cost satellite with even lower power can be achieved by restricting the use of heavy batteries which in turn reduce the total satellite weight. The ULP operation can be achieved by reducing the supply voltage to near threshold or sub-threshold region [1], [2], thereby significantly reducing static and dynamic power consumption. But, it has introduced serious reliability concerns to modern electronic systems that are susceptible to radiation effects than circuits powered at nominal supply voltages. Among them, SRAMs that are utilized in modern microprocessors for high speed computation gets affected a lot. These data-storing sub-systems occupy a significant area of the whole microprocessor chips and the area may increase for SoCs. Therefore, the leakage current of a memory contributes a large partition of its total power consumption. With this increased complexity of the microprocessors and digital signal processors, on-chip register files and SRAMs are expected to increase significantly while the high speed demand is insisted. The motivation of low voltage fault-tolerant memory design comes from two emerged requirements, ultra-low-power consumption, and Single-Event Upset (SEU) tolerance.

For very-deep-submicron technologies, lowering supply voltage have significantly reduced the critical charge of memory cells. This explains how the particles with lesser energy can flip memory cells, causing it sensitive to atomic particles from materials within the chip. SEUs also indicate the same phenomenon that the energetic particle hit, can generate a charge that causes a bit flip, if the charge is collected by sensitive regions of the circuit, can alter the logic value in that node temporarily [4], [5], [6]. In regenerative circuits like SRAM cell, this temporary voltage glitch can be fed back and ensures a bit flip. Thus SEUs may interpret as error when the charge collected (Q) at that node exceeds critical value (Q_{crit}) and results in logic state change. The charge deposited by a particle strike can be calculated from the integral of transient pulse and critical charge Q_{crit} is the minimum charge deposited in a sensitive node that results in memory bit flip [7].

However, SEUs can also occur in standard terrestrial environment at non negligible rates [9], due to the reduction of Q_{crit} with technology scaling [8]. Various solutions have been proposed to overcome these soft errors. Architectural solutions, such as error correction coding (ECC) and triple modular redundancy (TMR) [10], [11], are often not effective for small arrays in ULP systems operated at low supply voltages, due to their high complexity and the resulting performance penalty in memory requirements. Technology solutions, such as silicon-on insulator and other process techniques, can improve the data reliability but do not entirely solve the SEU problems, and often high volume manufacturing is not feasible [12]. Previously proposed bitcell solutions, such as the Dual Interlocked storage Cell (DICE) [13], are designed for super threshold operation and fail when operated at low voltages.

In this paper, a radiation tolerant 13T SRAM bitcell, designed for low- voltage operation, is proposed. It employs dual-driven separated-feedback mechanism to achieve robust SEU suppression, and is shown to tolerate upsets when operated at scaled supply. It has been designed in 180nm CMOS process using Tanner EDA schematic editor (S-edit) maintaining a unit cell size that is 2x larger than a standard 6T SRAM bitcell in the same CMOS process. Transient analyses were carried out using TSPICE to prove

functionality and upset tolerance and the waveform can be viewed in waveform editor (W-edit) were the performance parameters can be measured.

The paper is organized as follows. Section II describes the issue of SEUs in conventional 6T SRAM cells. Section III describes the design and architecture of the 13T bitcell. In Section IV, the radiation tolerance of the proposed bitcell is described, based on a unique self-correction mechanism, also it describes the 4x4 memory array with random injection of SEU using LFSR. Section V concludes this paper.

II. CONVENTIONAL 6T SRAM UNDER SEUS

As antecedently mentioned, SRAM blocks occupy the bulk of the chip space and are the first contributors to leakage power [14]-[16]. These trends cause two major conclusions. First, as a result of their static power consumption, scaling the supply voltage of the SRAM memory is an economical methodology to cut back total chip power. Second, the likelihood of a radiation strike on an SRAM bitcell is comparatively high as a result of the large area that the SRAM core occupies. Therefore, SRAM soft-error mitigation has become essential for sturdy system design.

The standard 6T SRAM bitcell utilizes a lively feedback loop between 2 cross coupled inverters so as to retain its stored value is shown in Figure 1. The cross coupled loop is incredibly sensitive to SEUs, as any upset that causes one of the data nodes to cross the shift threshold of the adjacent inverter will end in a bit flip. When operating at lower voltages, the switching threshold decreases, thereby increasing the soft-error susceptibleness of the circuit.

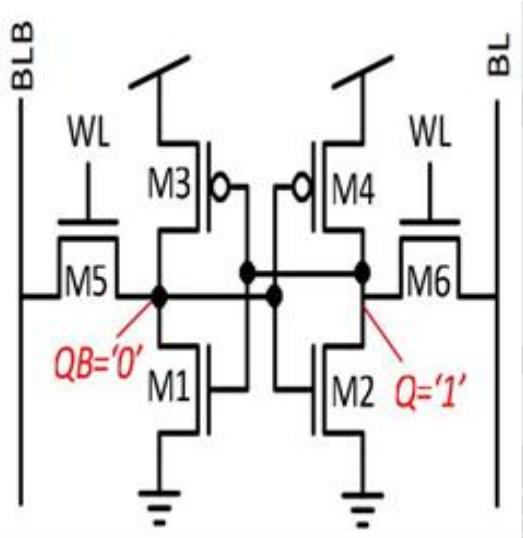

Fig 1.Conventional 6T SRAM bitcell

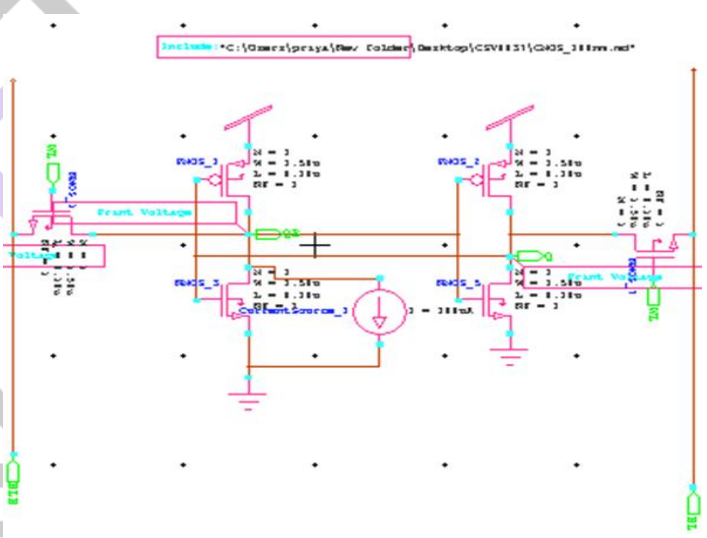

Fig 2(a). Schematic of 6T SRAM error bitcell

In the above structure of 6T SRAM bitcell, to write the data, the word line (WL) is made high with logic 1, so that data placed in the bit lines (BL and BLB) gets driven by transistors M5 and M6 to corresponding output nodes (Q and QB) respectively. To read the data from the stored nodes, the bit lines are precharged to $V_{dd}/2$. To demonstrate the 6T SRAM bitcell is susceptible to SEU failure, the following example will assume that an energetic particle strikes the circuit and induces a transient current pulse. The radiation modelled as current source that is injected to the sensitive node where the data gets stored is shown in Figure 2(a). Assume that data stored at Q = logic 1(V_{dd}) and QB = logic 0 (GND). When the energetic particle strikes a drain of the PMOS transistor (M3), a charge will be generated at that node, changing the state of output QB temporarily to logic 1. This type of charged strike leads to 0 to 1 upset referred as positively charged strike at QB, as opposed to a negatively charged strike referred to 1 to 0 upset at this node. The deposited charge can be evacuated to the power supply through the conducting transistor of the feedback inverter (M1), before the feed-forward inverter (M2 andM4) switches and discharges Q. In turn, this enforces the wrong state at QB, thereby latching the error into the memory cell.

The amount of charge needed to exceed critical charge is two orders-of-magnitude smaller than the deposited charge by an energetic particle strike in a high radiating environment. Since Q_{crit} gets decreased with voltage and technology scaling, it impairs the SEU tolerance of SRAM. Considering static noise margin as performance measure to analyse the stability of an SRAM cell [17] simulations were shown operated at 1V Fig 2(b). However, the generated charge by a particle can reach up to hundreds of femtocoulomb [4]. To overcome particle strike of such a magnitude, an alternative cell topology is considered stated as Radiation-Harden-By-Design.

III. THE PROPOSED RADIATION TOLERANT 13T SRAM BITCELL

A. Bitcell Design

For low voltage operation SRAM designs become popular in recent past. Alternative bitcell designs and architectural techniques have been proposed to enable operation in subthreshold region [15], [18] - [21]. These designs generally increase the number of transistors into the bitcell topology, compared to baseline 6T SRAM bitcell, trade-off density with robust, low-voltage

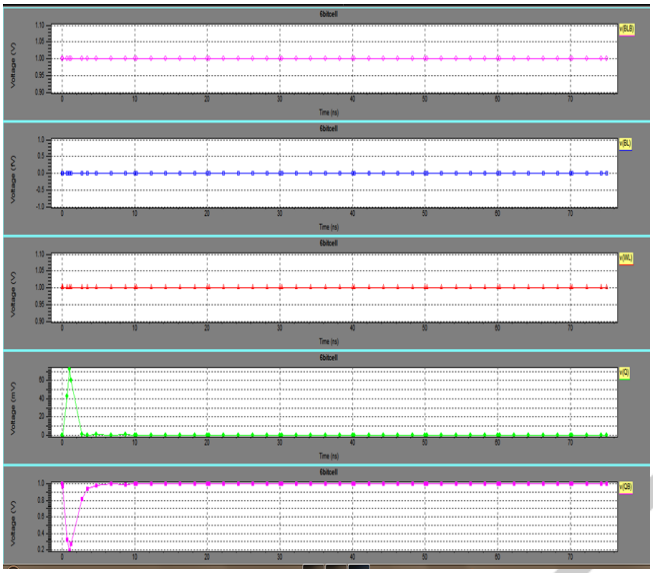

Fig 2(b).Output of error bitcell

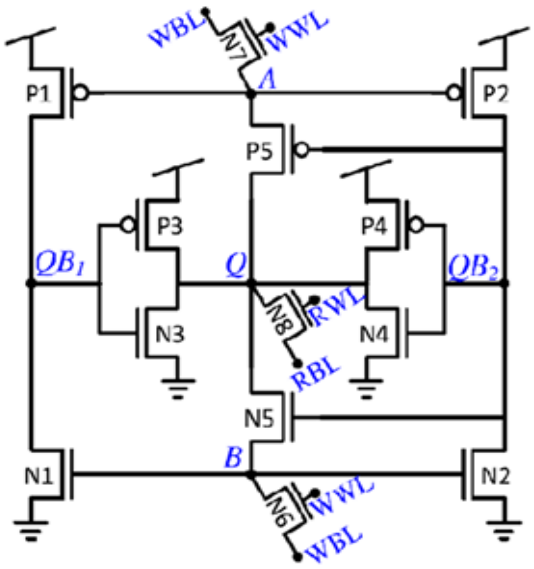

Fig 3.Schematic of proposed 13T radiation tolerant bitcell

functionality. However, robustness of 6T bitcell is extremely low, compared with alternative radiation hardening solution designs as shown in section II.

The proposed 13T SRAM bitcell is designed specifically for robust, low voltage operation in high radiating environments. This is achieved by employing dual-driven separated-feedback mechanism to improve susceptibility to soft error (SEU) due to supply voltage scaling in the design. The schematic of proposed cell design is shown in fig 3. The 13T bitcell has two stable states namely logic 1 and logic 0, defined as the voltage level at node Q. Similar to cross coupled inverted structure, inverted voltage will be stored at the internal data nodes. The storage mechanism of this circuit comprises five separate nodes: Q, QB1, QB2, A, B with acute data value stored at Q. This node is driven by pair of CMOS inverters (dual-driven separated-feedback) made up of transistors N3, P3, N4, P4 respectively, that are driven by inverted data levels stored at QB1, QB2. QB1 and QB2 are driven to V_{dd} or GND through transistors P1, N1 and P2, N2 that in turn controlled by weak feedback nodes A and B that are connected to Q by a pair of complementary devices (P5 and N5) gated by QB2. This setup protects Q from upset from the mechanism applied with node separation for SEU protection, having a high critical charge at node Q.

B. Write and Read Operation

In 6T SRAM bitcell, data was written directly by driving the new level in to the storage nodes, and therefore are required to overcome the circuit's strong internal feedback. In contrast to this design, the proposed design employs transistors (N6 and N7) connect a unified write bit line (WBL) to nodes A and B. These devices are controlled by a word line (WWL), such that when WWL is raised, nodes A and B are pulled towards the level driven upon WBL. The virtual connection between nodes A and B creates inverters (N1, P1 and N2, P2) driving QB1 and QB2 to the opposite level of WBL, accordingly the written data level is driven back to Q through feedback inverters, bringing the cell to stable state.

The proposed design has a separate read access transistor (N8) provides a single-ended readout. It is controlled by a separate read word line (RWL) and connected to a column shared bit line (RBL). It gets precharged prior to read operation and conditionally discharged based on stored voltage at Q. Q is driven to its stable value, due to dual-driven feedback and this read operation is more robust, faster than conventional SRAM design. In 6T SRAM, access transistor is stronger than pull-down transistor results in read failures. The 13T SRAM employs a pair of pull-down transistors (N3 and N4) that reduces the probability of read failure.

The previously proposed cells like 8T SRAM cell are susceptible to half-select failures. Such a situation occurs during write operations when some of the bits that share the same word line that are to be written. The 6T cells shares the word line and bit line for both read and write operation, biasing the bit line ensures that the cell will not be written to (during read operation). In scaled supply voltage operation read margin could be the limiting factor, so that single-ended readout is preferred as an alternative. In 13T bitcell, a half select situation will occur during a partial row write. However, the cell provides robust half select stability due to dual-driven feedback mechanism and indirect write operation through weak feedback nodes.

C. SEU Tolerance

The multiple internal nodes of the proposed 13T circuit provides better SEU tolerance and the possibility of strikes of both positive and negative polarities require an analysis to evaluate disrupt tolerance. As earlier said, a correct readout only requires the stable data to be at Q, therefore it is sufficient to consider voltage stored at Q for evaluation. The proposed cell has an inherent SEU tolerance ensured by two basic principles.

- Any temporary upset on other nodes can be tolerated, as the data are readout from node Q
- The assisting nodes are designed with redundancy to ensure that any upset will be mitigated by other nodes

When a radiation strike causes value change on any node of bitcell, the other four internal feedback nodes are designed to suppress the bit flip at this node within a deterministic recovery time. For example, an upset at Q will quickly be suppressed by the inverters through dual-driven feedback mechanism. Due to their separated nature, upsets at QB1 and QB2 will not be able to change the state at Q and will return to their original state.

D. Modeling Radiation as a Current Source

The methodology commonly used to study transient effects as SEU will couple the SPICE simulations with current injection. The current pulse is extracted from different kind of simulations or more often modelled. Then this current is injected as a current source by passing the drain and bulk electrodes of the sensitive transistor of the SPICE-modelled SRAM. Radiation dose produces an electron-hole pairs that results due to drift and diffusion upset of the device. This nature of the dose is represented by current source in double exponential form, with rapid rise time (t_r) and gradual fall time (t_f) connected at the sensitive node. Let Q_{inj} be the total charge deposited by the current pulse, K is the charge deposited along a unit length of ionizing particle track, L_c is the charge collection depth and LET is the linear energy transfer in (Mev-cm2)/mg.

$$I_{inj}(t) = Q_{inj} * T_W \quad (1)$$
$$Q_{inj} = K * L_c * LET \quad (2)$$
$$T_W = [e^{(-t/tf)} - e^{(-t/tr)}]/(tf-tr) \quad (3)$$

Normally $t_r << t_f$ due to the slow decay of ion track and has a typical value of ~200ps. Injected current variation for different LET values for t_r=50ps, t_f=164ps, K=10.8, Lc=2μm and T_w a constant current pulse width.

E. Block Diagram of SRAM Memory Array

SRAM memory array includes address decoders to locate the data in a particular bitcell, write circuitry, sense amplifier circuitry and precharge systems. The block diagram of memory array is shown in Figure 4. The SRAM write circuitry connects directly to the bit lines and is used to write a value to the SRAM cell. The value stored in the SRAM cell is stored at node Q, while the inverse of the value is stored at node QB1 and QB2.Input and output buffers should latch the data in the buffer during read operation and be switched off during write operation. In addition, the buffer should have enough drive capacity to obtain a reasonable speed at sub-threshold voltages. This concern of sub-threshold drive capacity imposes an additional requirement for this data buffer design.Address decoding is the process of generating chip select signals from the address bus for each device in the system. Address decoders are of two types row and column address decoders controlled by row and column address select line. An address decoder is a binary decoder that has two or more inputs for address bits and one or more outputs for device selection signals. When the address for a particular bitcell appears on the address inputs, the decoder asserts the selection output for it.

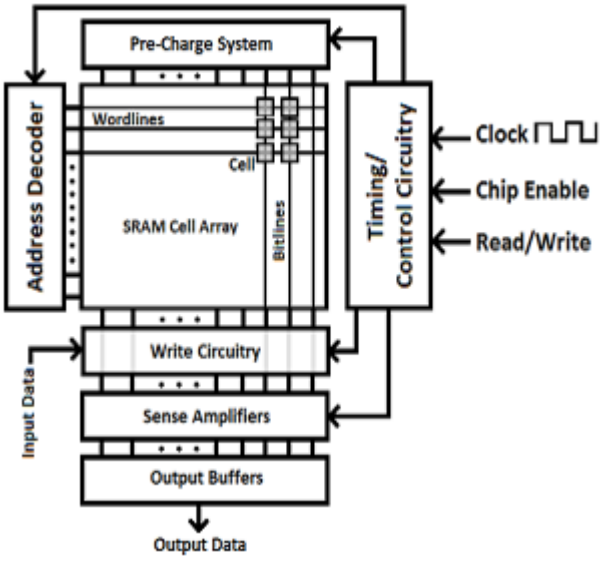

Fig 4.Block Diagram of SRAM memory array.

IV. Results and Discussions

A. Disrupt Radiation Tolerance 13T SRAM Bitcell

In the proposed 13T SRAM bitcell, when the energetic particle strikes the sensitive node it induces the transient current pulse $I_{inj}(t)$, that is modeled as double exponential current [23] by a fast rise time and gradual fall time on a reverse-biased junction. On an unbiased condition, the generated e-h pair will spontaneously recombine and not induce a current pulse due to absence of electric field.

With a V_{dd} = 1V and an exponential current pulse is induced at QB1 is shown in Figure 5(a) and the corresponding results is shown in Figure 5(b).

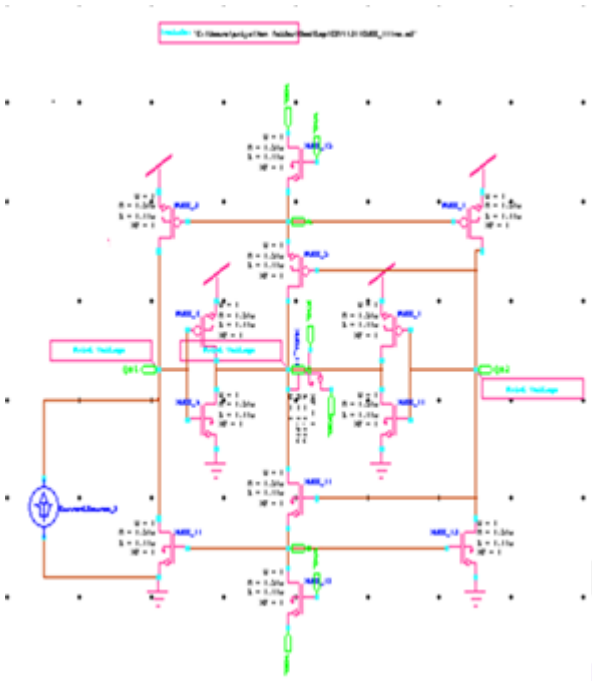

Fig 5(a).Schematic of 13T error bitcell

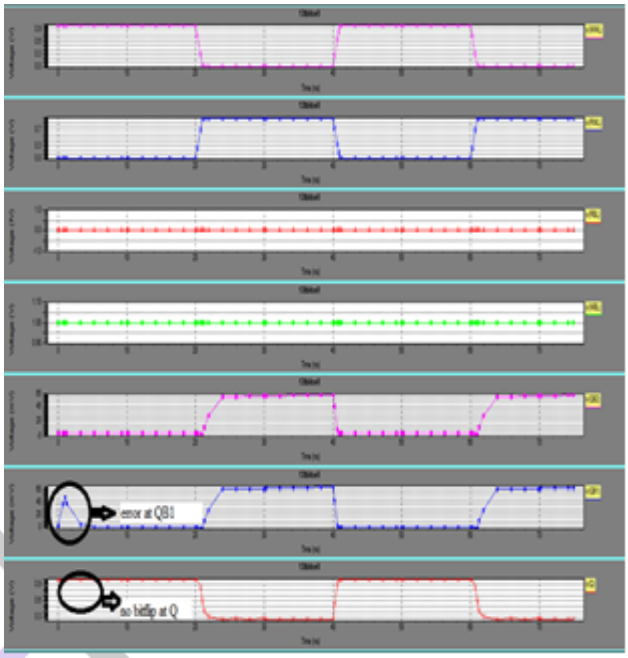

Fig 5(b). Output of 13T error bitcell

From the output shown in Figure 5(b), error at node QB1 (0 to 1 upset) has no impact on critical node Q (remains stable) protected by other internal node QB2. Thus the proposed design is radiation hardened compared to conventional designs. The comparison for critical charge analysis is shown in table 1 for proposed bitcell. For currents like 1mA, 5mA charge deposits get increased that affects the charge(data) stored in Q. But recovery mechanisms successfully enable the cell to recover and retain its initial state for every possible upset, though QB1 will not be in original state.

Table 1. Critical Charge Analysis

Current induced	Critical charge storage
100uA	577.3fC
500uA	2.83pC
1mA	5.74pC
5mA	28.73pC

B. 4X4 Memory Array using 13T bitcell using LFSR

The 4x4 memory arrays was designed with 13T SRAM bitcell along with sense amplifier and write buffer circuit for read and write operation in the memory array. Linear feedback shift register (LFSR) is used to randomly inject the error in the memory array at the nodes QB1 and QB2. The schematic of the memory array and a 4-bit LFSR designed is shown in Figure 6(a) and its corresponding output is shown in Figure 6(b). The output shown has error in the memory cell at the node Q5, but the node Q is free from it, as it gets protected by the other internal nodes through dual-driven mechanism. As LFSR is a random pattern generator it generates pattern in a random manner and the output of each register is connected to the corresponding cell in the array to either QB1 or QB2 thus it induces error in the bitcells present in the array.

When node Q is at logic 0, both QB1 and QB2 remains high. A positive particle strike on node Q will quickly discharge the injected charge through N3 and N4. During this upset event, B starts to charge through transistor N5, enabling transistors N1 and N2 to discharge QB1 and QB2. Since, P5 remains in cutoff region, A is at logic 0, causing P1 and P2 to combat the discharge of QB2 and QB1 until the charge injected to Q has been discharged.

When the negative particle strike at node Q, while holding the logic state 1 both QB1 and QB2 remain low, quickly replenishing the lost charge at Q through transistors P3 and P4. During this upset A discharges through P5, enabling P1 and P2 to

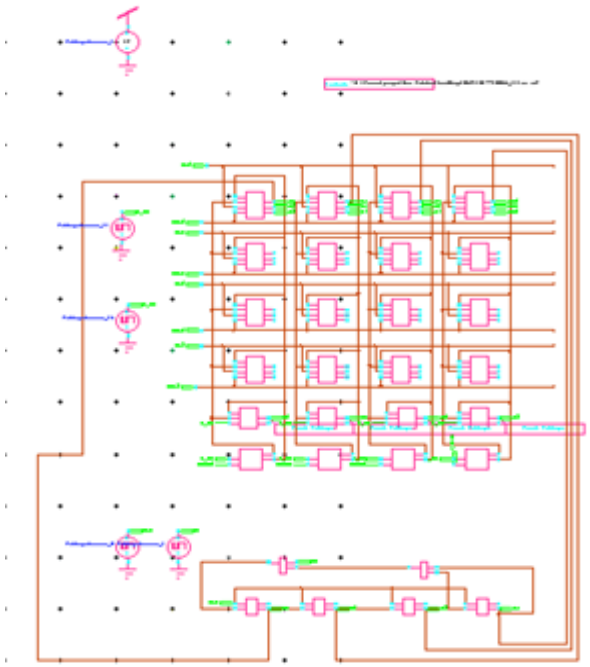

Fig. 6(a).Schematic of 4x4 memory array with LFSR

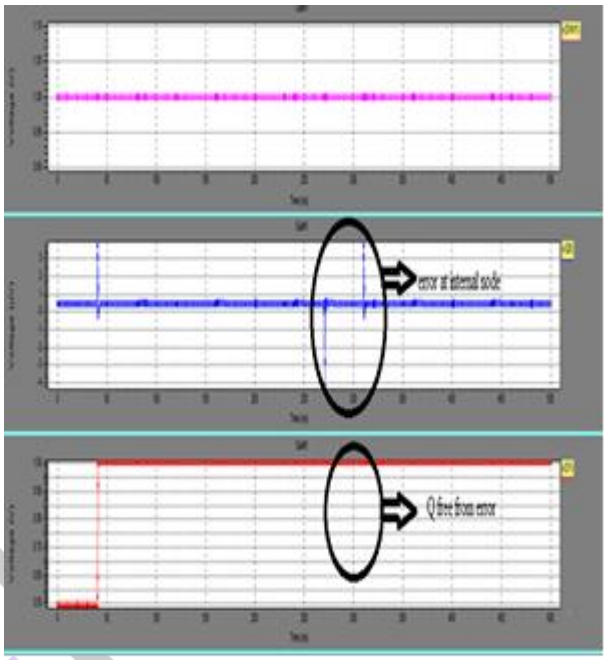

Fig. 6(b). Output of 4x4 memory array with error at node Q5

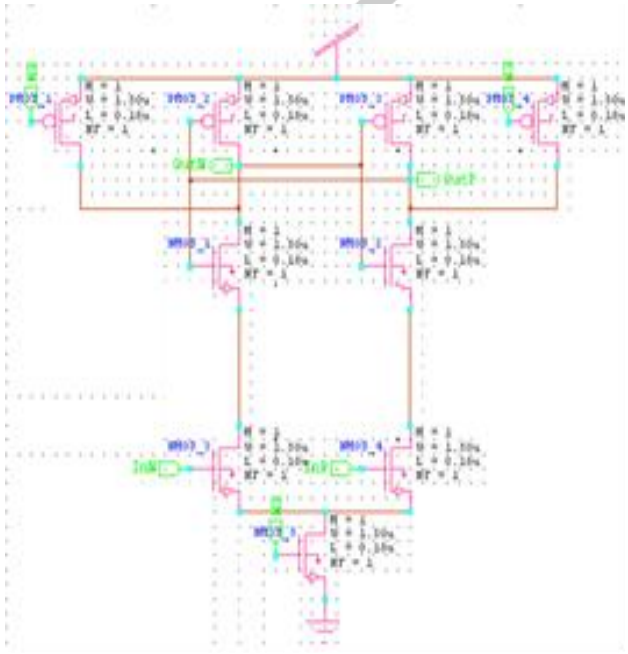

Fig. 7(a).Current controlled latched sense amplifier

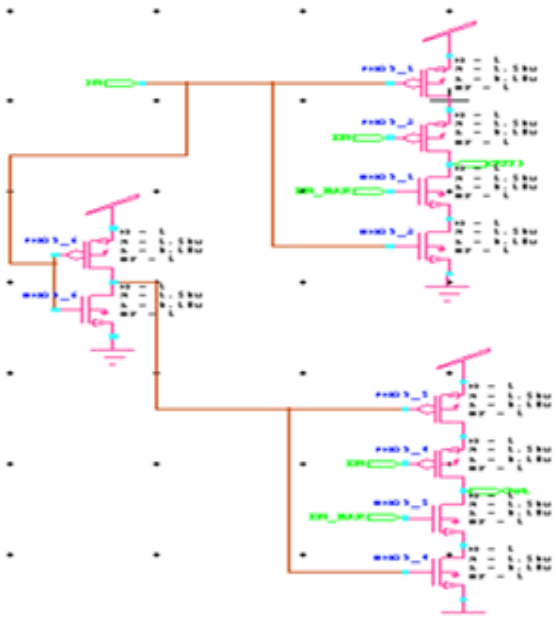

Fig. 7(b). Write Buffer circuit

C. Sense Amplifier and Write Buffer Circuitry

The voltage sense amplifier is the current controlled latched sense amplifier. It combines the aspects from both latch based voltage mode sense amplifier and the differential pair amplifier is shown in Figure 7(a). The amplifier uses the latch based design, has the bit lines attached to the transistors N3 and N4. This results in high input impedance that decouples the bit lines from the output. The transistors N1, P1 and N2, P2 form the two inverters. When the amplifier is off, the signal SE is at logic 0. This turns on the reset transistors P3 and P4, clearing the previous latched value and holding the latch at its metastable point. The bit line inputs are connected to the gates of MOSFETS N3 and N4. When the sense amplifier is enabled, the reset transistors turn off, and the current source N5 turns on, causing an even current flow through each half of the amplifier. The bit line that is discharging causes the gate voltage to drop, which decreases the current flowing through that side of the amplifier and causes the voltage to rise. This will cause the amplifier to latch, which will stop the static flow of current and display a valid value at the output.

The data can be written to the cell through the write buffer circuit shown in Figure 7(b). , that has true and complementary outputs for both bit line (BL) and bit line bar (BLB).

V. Conclusion

The proposed 13T SRAM bitcell is designed for robust, low-voltage operation in high radiation environments. It displays a dual-driven separated- feedback mechanism to achieve high soft error tolerance with the scaled voltage down to 1V. It tolerates the upsets with the charge deposits of 500fC. The cell provides better immunity to soft errors when compared to 6T SRAM cell. A 4x4 memory macro was designed and tested using LFSR showing read and write functionality. The techniques were implemented to decrease SEU probability, while maintaining a bitcell area much smaller than alternative solutions, such as previously proposed TMR, resulting in a unit cell area 2x larger than a standard 6T bitcell in a same 180nm process. To reduce this area overhead it can be designed using other process technologies like finFET where recent VLSI researches are going on these technologies to reduce these difficulties.

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