A DVR Implementation for Harmonic Compensation in Distribution Systems by using Series Voltage source Inverter

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***Abstract*—Dynamic voltage restorers (DVRs) are now becoming more established in industry to reduce the impact of voltage sags to sensitive loads. However, DVRs spend most of their time in standby mode, since voltage sags occur very infrequently, and hence their utilization is low. In principle, it would be advantageous if the series-connected inverter of a DVR could also be used to compensate for any steady-state load voltage harmonics, since this would increase the power quality "value-added" benefits to the grid system. However, before this can be done, consideration must be given to the control of steady-state power through the DVR, the increased losses, and the low modulation depths at which the scheme must operate to achieve acceptable harmonic compensation performance. This paper presents a selective harmonic feedback control strategy that can be easily added to medium-voltage DVR systems to provide voltage harmonic compensation capabilities with minimal effect on the sag compensation performance of the basic DVR.**

Series voltage inverter operation is controlled by multiple pulse width modulation. The output of the Series voltage Source inverter is controlled by using pulse width modulation, generated by comparing a triangular wave signal with an adjustable DC reference and hence the duty cycle of the switching pulse could be varied to synthesize the required conversion. DVR can be considered to be cost effective when compared with other compensation devices. But the use of DC link capacitor in the conventional DVR will increase the size, weight and the cost of the entire system which inhibits widespread use of DVR The dynamic voltage restorer is one of the modern devices used in distribution systems to protect consumers against sudden changes in voltage amplitude. The simulation results are obtained using MATLAB/SIMULINK software.

***Index Terms*—Active filter, dynamic voltage restorer, harmonics, medium voltage, series transformer, stationary frame control.**

I. INTRODUCTION

Dynamic voltage restorers (DVRs) are now becoming more established in industry to reduce the impact of voltage sags to sensitive loads [1]–[3]. However, since voltage sags generally only occur a few times each year at any particular location, a DVR system will generally spend most of its time in standby mode waiting for a sag to occur. Unfortunately, however, it will still introduce extra impedance to the line, primarily due to the series transformer, and this impedance will(in turn) cause a voltage drop to the load and increased load voltage harmonics when nonlinear loads are present [4].In principle,

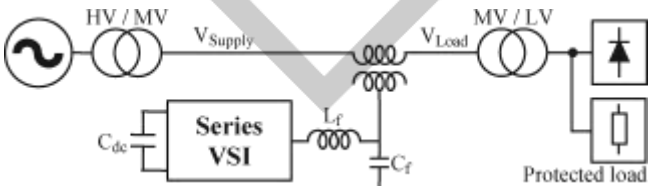
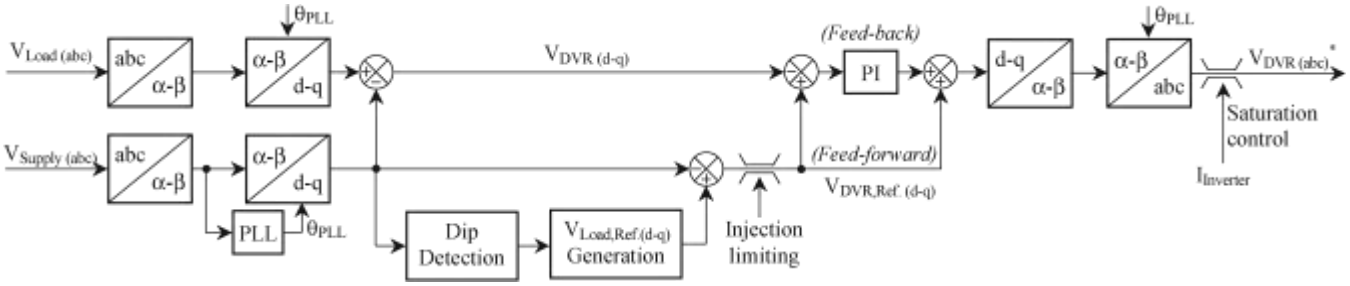


Fig. 1.Series topology of the DVR.

This would increase the power quality "value-added" benefits to the system (which is the definition and driving force of custom power applications) with minimal extra capital cost, but, of course, with some increase in inverter steady-state losses. The limitations in achieving this objective are steady-state power flow constraints and the low modulation depths that must be used with a DVR that has a typical voltage injection capacity. Fig. 1 shows a typical DVR series-connected topology, with a short-term energy storage capability (such as a capacitor bank or batteries) to ride through a voltage sag. Hence, most DVRs cannot supply significant steady state real power and also can absorb almost no steady-state real power back through the series connection. Therefore, any steady-state harmonic voltage compensation strategy that is implemented must ensure that the steady-state real power flow through the DVR is kept close to zero.

The typical voltage injection capability of a DVR is around 50%. Hence, to compensate for harmonics as low as 1% (or lower), the system must operate at modulation depths of around 2%; but high magnitude and phase accuracy must still be maintained for the compensation to be effective. Recent work [5] has proposed a feedforward approach for voltage harmonic compensation that also accounts for the sample delay and voltage drop across the filter inductance. However, this approach has only been verified by

simulation, and for practical systems, it is unclear how errors in the system at low modulation depths [e.g., parameter variations,



dead-time effects, pulse width modulation (PWM) counter resolution, calculation errors, quantization effects, and the presence of the series injection transformer] could affect the performance of this strategy.

In contrast, this paper presents a selective harmonic feedback control strategy that can be easily added to medium-voltage DVR systems to provide voltage harmonic compensation

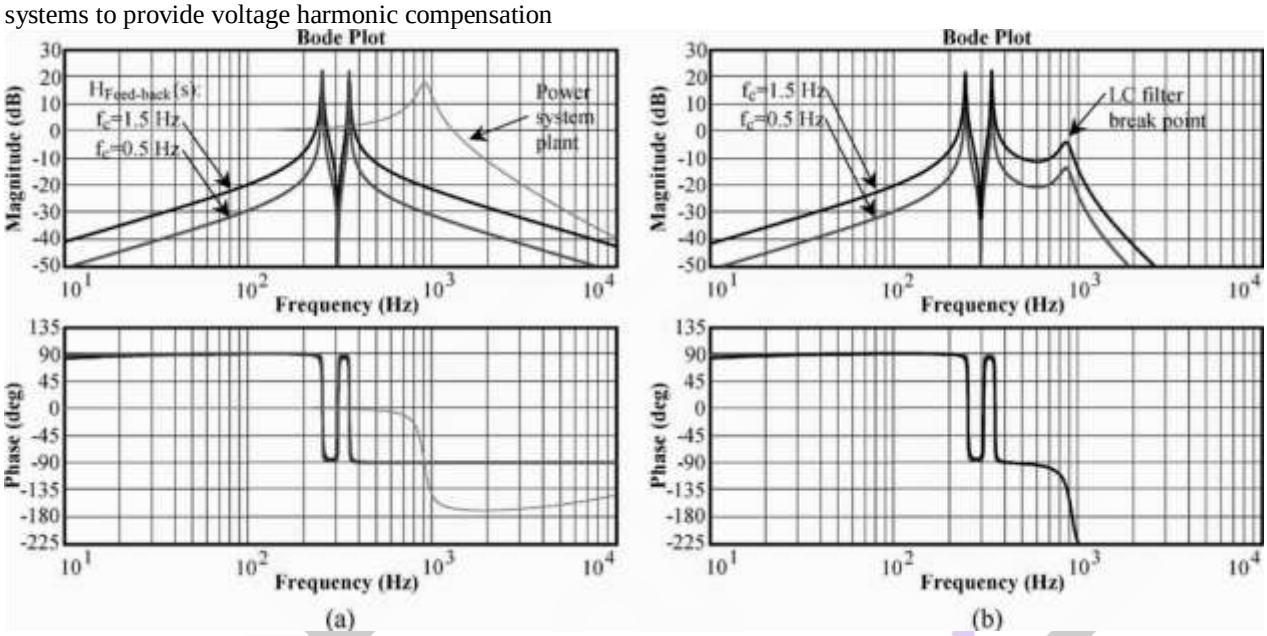


Fig. 3.Simulated open-loop frequency response of the (a) separate feedback controller [i.e. $H_5(s) + H_7(s)$] and power system plant and (b) full system
(i.e. feedback controller and power system plant).

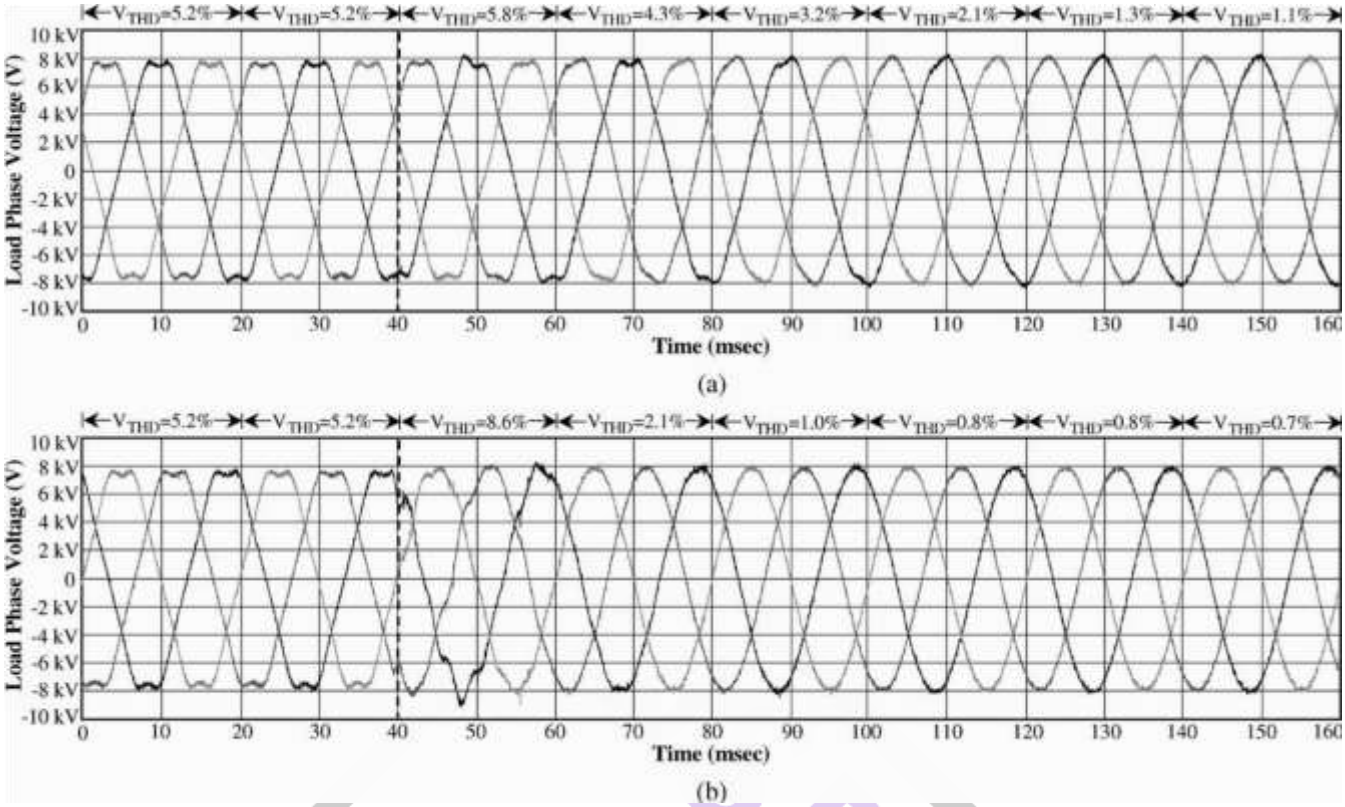
Capabilities with minimal effect on the sag compensation performance of the basic DVR. The proposed controller has been experimentally verified on a medium-voltage (10 kV) three phase DVR prototype under a range of conditions, including distorted supply voltages, nonlinear loads, and operation during distorted voltage sags. A brief introduction to the controller of a conventional DVR is first presented, followed by discussion and verification of the proposed new harmonic compensation controller.

I. CONTROL OF THE DVR

A. Existing Sag Compensation Control

The primary existing control structure for a typical DVR sag compensation system is based on a combination of supply voltage feedforward and a polarization index (PI) *d*−*q* load voltage feedback (Fig. 2). A software-based phase-locked loop (PLL) is used to create *d*−*q* coordinate sinusoidal references from the supply, which are used to determine the target phase of the output voltages. The phase of these references is controlled to only vary slowly during transients from their presage values to minimize phase jump effects. The feedforward control then calculates the appropriate modulation depth to inject compensating voltages between the supply voltages (V_{Supply}) and the load voltages (V_{Load}) to restore the load voltages to the target references. However, this does not account for the voltage drop across the filter inductor and other parameters such as the transformer, and, hence, closed loop load voltage feedback control is then added in the *d*−*q* frame to minimize any SteadyState error in the fundamental component.

When the grid voltage is normal, the DVR system is held in a null state to lower its losses. When a voltage sag is detected, the DVR switches into active mode to react as fast as possible to inject the required alternating current (ac) voltages between the grid and the load. The sag detection strategy is based on the root mean square (rms) of the error vector, which allows for the detection of symmetrical and non-symmetrical sags as well as any associated phase jump.



B. Proposed Additional Selective Voltage Harmonic Compensation Control

To add voltage harmonic compensation to the DVR system, the inverter must now switch continuously, instead of only when sags occur. Therefore, the standby mode must be revised to accommodate this change. For most DVR systems, this will have little effect on the device conduction losses, but the additional switching losses must be traded against any power

Fig. 4.Experimentally measured startup transient response of the voltage harmonic compensation controllers (*t*start = 40 ms).

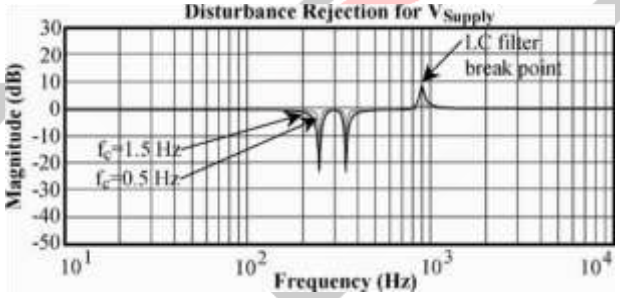


Fig. 5. Simulated supply voltage disturbance rejection from the load voltage due to the proposed harmonic controllers.

Quality savings and possible reduction in downstream line and load losses by virtue of the reduced harmonics.

As identified before, it is critical that the harmonic compensation scheme has a net real power flow of zero (or very close to zero) at all times. Otherwise, since the system only has a small rated unidirectional power supply, a net power flow out of the inverter will deplete the available energy stored in the capacitors, and a net power flow into the inverter will increase the direct current (dc)-bus voltage past its ratings and possibly damage the system. To minimize the net real power flow, narrowband resonant-based controllers [6] are used to compensate for each selected harmonic, with no proportional term. Resonant controllers were used instead of synchronous frame *d*−*q* integral controllers at each frequency due to the significant computational advantages that are achieved when stacking multiple controllers, their single-phase usage options,

TABLE I MAIN SPECIFICATIONS OF THE EXPERIMENTAL DVR

PARAMETER	VALUE
Nominal grid voltage	V_{Supply} = 10 kV (l-l)
Nominal load voltage	V_{Load} = 380 V (l-l)
Max. series voltage injection	V_{DVR} = 5 kV (l-l)
Max. series power injection	S_{DVR} = 200 kVA
Switching/sampling frequency	f_{sw} = 5.0 kHz
Max. inverter dc-bus voltage	V_{DC} = 600 V
Capacitance of dc-bus	C_{DC} = 26 mF
Filter inductance	L_f = 260 µH
Filter capacitance	C_f = 120 µF

And also due to their combined positive and negative sequence compensation [7], [8]. Fig. 3(a) shows the frequency response of the stacked fifth and seventh resonant controllers, which have a high attenuation of any 50-Hz components to minimize disruption to the sag compensation system and the real power flow. Furthermore, it should be noted that any small 50-Hz component left in the controllers will be phase shifted by approximately 90°, and will, therefore, in any case, only demand reactive power (again having no effect on the real power flow). The resonant control filter from [6] can be rewritten as

$$H_n(s) = 2K_I\omega_c \frac{s+\omega_c}{s^2+2\omega_c s+\omega_n^2+\omega_c^2} \quad (1)$$

Where$_{KI}$is the gain at the selected frequency, irrespective of the chosen cut-off frequency ω_c, and $\omega_n$is the selected harmonic

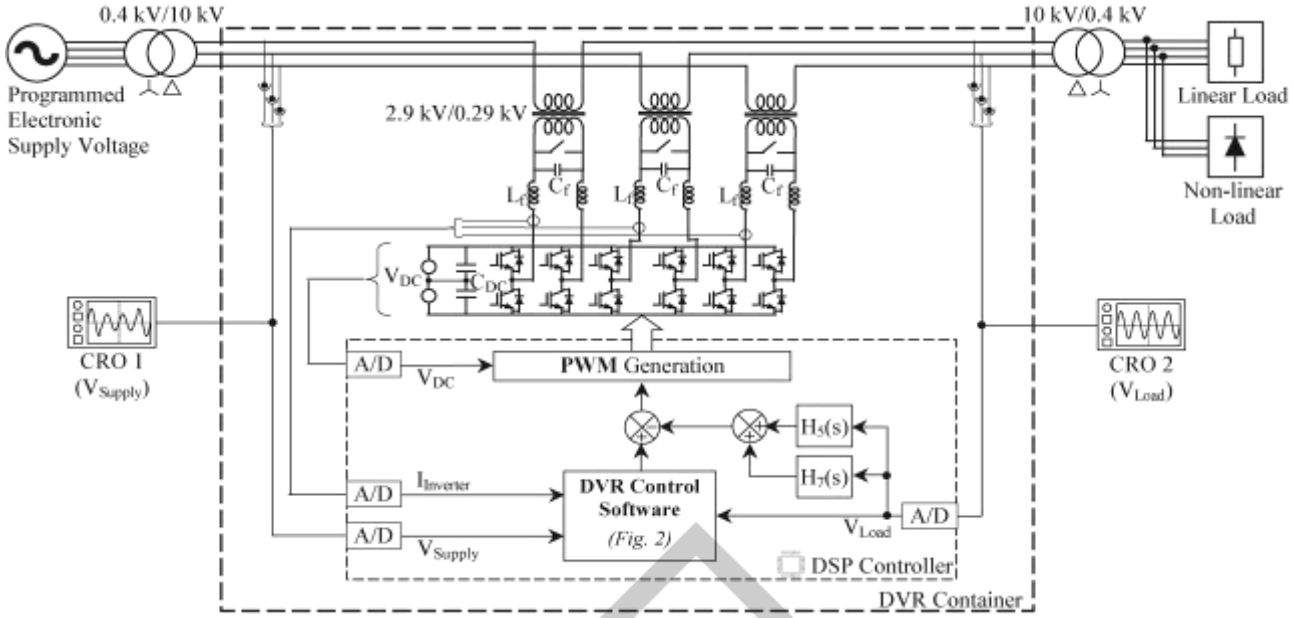


Fig. 6.Circuit and control block diagram of the DVR (placed in a 20-ft container) and the experimental power system test setup.

Fig. 7. Photo of the DVR container and the 10-kV/0.4-kV distribution transformers for the test supply and load.

Frequency. The full harmonic feedback controller is, therefore, given by

$$H_{\text{Feedback}}(s) = \sum_{n \in N} H_n(s), \quad \text{where } N = \{5,7\}. \qquad (2)$$

Changing the value of ω_c provides a compromise between the transient harmonic performance and selectivity of the controllers. The change in selectivity is illustrated in Fig. 3(a) for f_c values of 0.5 and 1.5 Hz (i.e., $\omega_c = 2\pi f_c$). As the resonant spike widens, the surrounding gain also increases; this, in turn, provides the improved transient response. However, the expected disadvantage of the improved performance of the higher cut-off value is a reduction in stability. This can be seen in Fig. 3(b), with a gain margin drop from 14.3 to 3.8 dB with f_c set to 0.5 and 1.5 Hz, respectively.

Fig. 4 presents the experimentally measured start up transient responses for both values of f_c (refer to Section III for experimental details). The response in Fig. 4(a) (i.e., f_c = 0.5 Hz)

TABLE II

EXPERIMENTAL RESULTS AND LOAD VOLTAGE HARMONICS BEFORE AND AFTER SERIES COMPENSATION

Harmonic Source	Voltage Measurement	5th	7th	THD
(a) Supply Voltage Distortion	V_{Supply}	4.7%	2.1%	5.2%
	V_{Load}	**0.4%**	**0.1%**	0.7%
(b) Non-linear Load	V_{Supply}	1.1%	1.0%	1.7%
	V_{Load}	**0.1%**	**0.1%**	0.9%
(c) Supply Voltage Distortion and Non-linear Load	V_{Supply}	5.8%	3.1%	6.7%
	V_{Load}	**0.5%**	**0.3%**	1.2%

is much slower than that in Fig. 4(b) (i.e., f_c = 1.5 Hz), with settling times of five and two cycles, respectively. The reduced stability margin of the 1.5-Hz version is well illustrated by the large injection overshoot of the first settling cycle in Fig. 4(b).

The disturbance rejection simulation of the voltage harmonic controllers is illustrated in Fig. 5, where the disturbance is taken as the supply voltage (V_{Supply}) and the target is the load voltage (V_{Load}). This shows that the controllers have virtually no effect on the fundamental voltage, have more than 20 dB of attenuation of the fifth and seventh selected harmonics, but also have a small effect on supply disturbances around the break point of the inductance–capacitance (LC) filter. At this point, the 1.5-Hz controller has the higher disturbance gain of 8 dB, whereas this gain is less than 2 dB for the 0.5-Hz controller.

The resonant controllers were implemented using delta operator-based infinite impulse response (IIR) second-order digital filters to ensure high accuracy. To further improve the performance of the resonant filters, the sample delay (d_{elay})

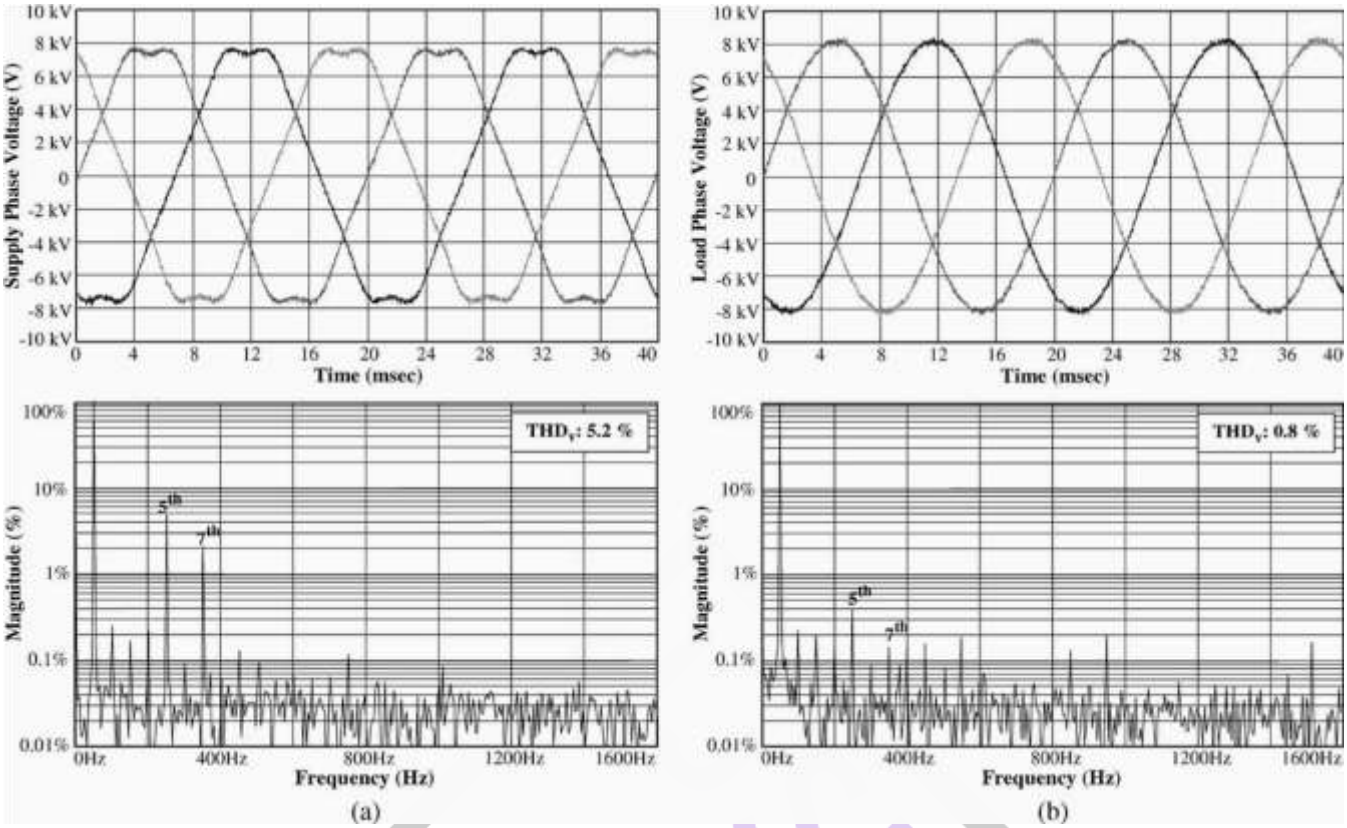


Fig. 8. Experimentally measured steady-state voltage harmonic compensation performance: Linear load. (a) Supply voltage (fifth = 4.7%; seventh = 2.1%). (b) Compensated load voltage (fifth = 0.4%; seventh = 0.1%).

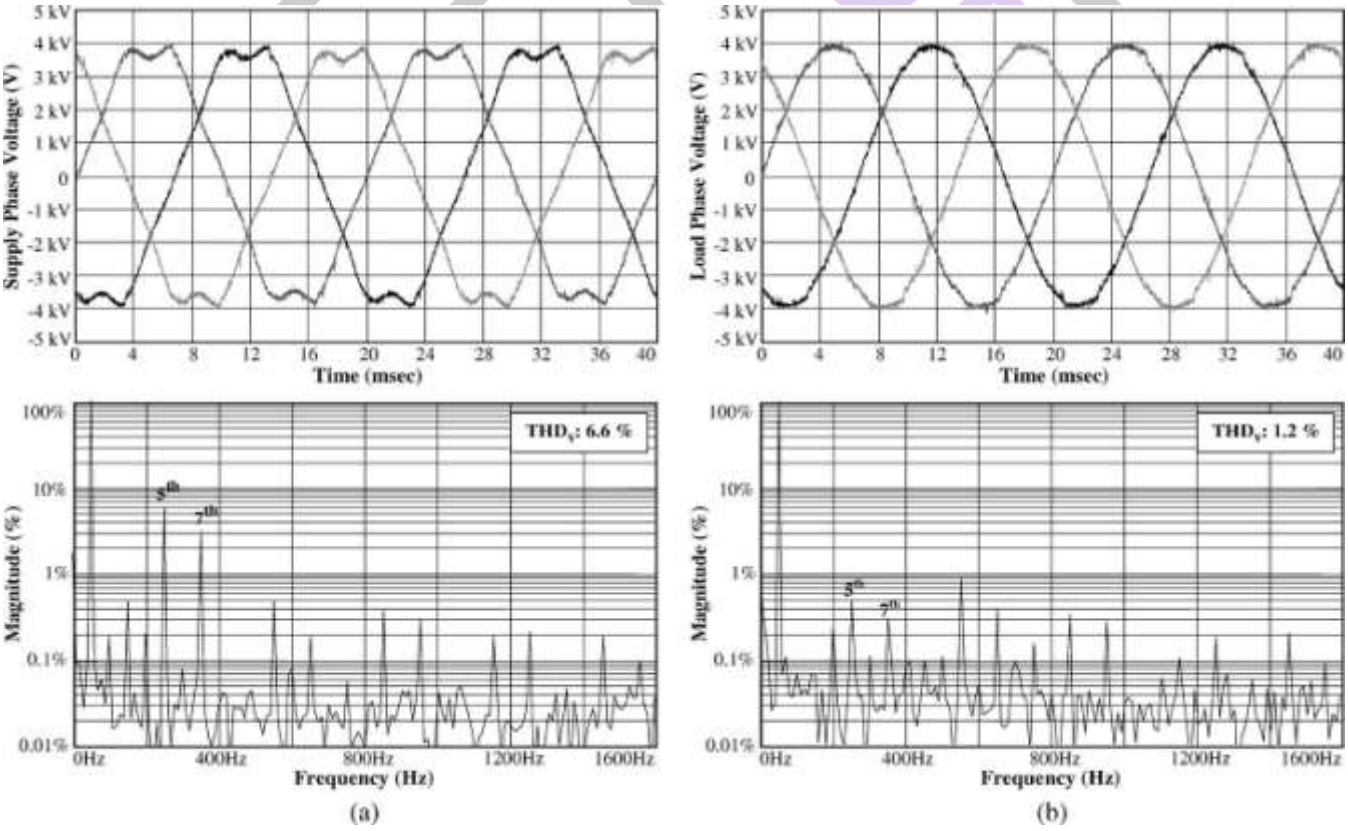


Fig. 9. Experimentally measured steady-state voltage harmonic compensation performance: Nonlinear load. (a) Supply voltage (fifth = 5.8%; seventh = 3.1%). (b) Compensated load voltage (fifth = 0.5%; seventh = 0.3%).

of each discrete controller was separately compensated (since each harmonic is controlled separately) [8] as

$$H_n(s) = 2K_I\omega_c \frac{\cos\phi_n s + (\omega_c \cos\phi_n - \omega_n \sin\phi_n)}{s^2 + 2\omega_c s + \omega_n^2 + \omega_c^2} \quad (3)$$

Whereφn= $\omega n\tau$Delay.

II. EXPERIMENTAL TEST SETUP AND RESULTS

Table I provides the specifications for the digital signal processor (DSP)-controlled 10-kV DVR platform used for this work (refer to [4] for full details), with the schematic of the test setup provided in Fig. 6.

The medium-voltage prototype DVR was fed with a programmable California Instruments Supply at 380 V, which was then fed into a distribution transformer (see Figs. 6 and 7) to create the 10-kV line voltage. Three specially made 67-kVA 0.29 kV/2.9 kV single-phase series injection transformers are used to series connect the DVR's 200-kVA low-voltage inverter to the system. The load voltage was stepped down using another distribution transformer to allow low-voltage linear and nonlinear loads to be utilized. The dc bus of the inverter was charged to 600 V using a unidirectional dc supply, which provided 4680 J of energy in the 26-mF dc capacitors for transient use in the DVR's sag ride-through capabilities.

The nonlinear load was a diode rectifier with a parallel resistive/capacitive dc load. All tests were conducted at low power (a few kilovolt amperes) due to limitations on the programmable supply power at the time of the tests. While a majority of the tests were undertaken with a line voltage of 10 kV (i.e., 5.8 kV phase voltage), tests containing the nonlinear loads with high current peaks were conducted at only 5 kV, once again due to limitations in the supply. A 20-ft shipping container (Fig. 7) was used to house the medium-voltage DVR (including injection transformers, inverter, and controller) to allow relocation of the system for off-site testing.

An Analog Devices AD21062 floating-point Sharc DSP was used to implement the control algorithm shown in Figs. 2 and 6, with the PWM signal generation for the six insulated gate bipolar transistor (IGBT) phase legs created using a Siemens SAB 80C167 Micro Controller. The harmonic compensation was successfully tested at both 3 and 5 kHz, although space limitations allow only the 5-kHz results to be presented here. Note also that since symmetrically sampled PWM was used, the controller's sample rate is equal to the switching frequency. The medium-voltage supply and load voltages required by the controller were measured with ABB resistive voltage dividers and isolation circuitry.

The proposed controller was tested under steady-state and transient (i.e., voltage sag) conditions to both show the harmonic compensation performance of the system and to show that the performance of the DVR was not affected. A combination of results using both 0.5- and 1.5-Hz cut-off frequencies is used to allow comparison of the two situations (for transient results in particular). These results follow.

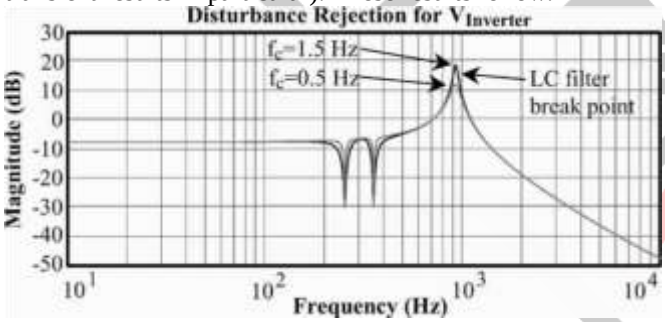


Fig. 10. Simulated inverter output voltage disturbance rejection from the load voltage due to the proposed harmonic controllers.

A. Steady-State Harmonic Compensation Tests

The steady-state performance of the proposed system is summarized in Table II, and includes results from: (a) a distorted supply voltage; (b) a nonlinear load current (which, in turn, creates a distorted supply voltage); and (c) a combination of the two (i.e., both distorted supply voltage and a nonlinear load). Figs. 8 and 9 show waveforms and frequency spectrums of the supply and load phase voltages for test setups (a) and (c), respectively. In all cases, the selected fifth and seventh harmonics are significantly reduced by a factor of 10 (i.e., 20 dB) or more, and the total harmonic distortion (THD) is also substantially reduced since these harmonics are the most dominant in the system. Note that compensation has only been incorporated for the fifth and seventh harmonics in this system, and other higher order harmonics will still exist. This can be seen in Fig. 9, where the fifth and seventh voltage harmonics are attenuated in the load voltage, but the other low-order harmonics such as the eleventh and thirteenth still remain. (Note that shifting to an asymmetrical PWM scheme would double the controller bandwidth and would allow these higher harmonics to be easily compensated using the same switching frequency [7]. In Fig. 8, an introduction of some small-magnitude harmonics can be seen in the load voltage (i.e., they do not exist in the supply voltage). During the experimental testing of the DVR under a variety of conditions, harmonics in the 800–1000 Hz range were consistently found to appear. While these harmonics were generally only in the order of 0.1%–0.3%, the effectiveness of the fifth and seventh compensation meant that in many cases, these harmonics became more dominant in the overall load vo.Since this frequency region contains the break point of the LC filter, it seems logical to conclude that the primary reason for the increase is LC filter resonance, especially since

Fig. 5 has already shown the expected amplification of supply voltage harmonics in this frequency region. However, correlating the disturbance plot in Fig. 5 with the seventeenth and nineteenth harmonics existing in the supply voltage does not match the magnitude of the load voltage harmonics found. Another source of excitation for this resonance must, therefore, exist. This source may well be the harmonics generated by the output of the symmetrically sampled PWM switching scheme.

B. Dynamic Sag and Harmonic Compensation Tests

The dynamic tests on the system were conducted using simultaneous harmonics and sags (symmetrical and asymmetrical) and included combinations of distorted supply and linear/ nonlinear loads as per the steady-state tests. During the transient events, the combined feedforward/feedback controller shown in Fig. 2 is enabled, and, hence, the system characteristics are changed. In particular, the added feedback proportional component provides some damping of the *LC* resonance. The control and disturbance plots that apply during transient events, therefore, vary from those provided earlier.

Fig. 11 shows the response of the DVR to a 0.79 per unit (p.u.) symmetrical sag and a linear load, with the harmonic compensation enabled. The sag compensation scheme can be seen to continue to function as expected, and the harmonic compensation settles within about two fundamental cycles with an f_c of 1.5 Hz. Note that as a part of the sag, the harmonic magnitudes will also typically vary, and, hence, the transient seen in the harmonic compensation. As with the previous start up transient [Fig. 4(b)], a small overshoot is seen during the first fundamental cycle when the larger value of f_c used.

Fig. 12 shows results for the compensation of another symmetrical sag, but this time with a nonlinear load. For these results, a smaller f_c of 0.5 Hz is used to allow comparison with the previous results. The response time to the transient is visibly slower, but has no initial overshoot. Note that as with the steady state results in Fig. 9, some harmonics still remain as only the fifth and seventh harmonics are targeted for selection.

The final results in Fig. 13 are for an asymmetrical sag with a linear load. At the low-voltage terminals of the programmable supply a 0.63 p.u. single-phase sag was created, which became a shallower two-phase sag on the medium-voltage side of the star–delta transformer. Once again, the sag is compensated as required, with a small harmonic overshoot created due to the 1.5-Hz cut-off frequency used for this result.Due to disturbance rejection differences between the 0.5and 1.5-Hz implementations around the break point frequency, the THD varies slightly between the two alternatives. However, since the compensation of the selected fifth and seventh harmonics is primarily controlled by the gain, little difference is seen between the two variations at these harmonics for a given gain condition. This result is also verified by both of the disturbance plots (i.e., Figs. 5 and 10).

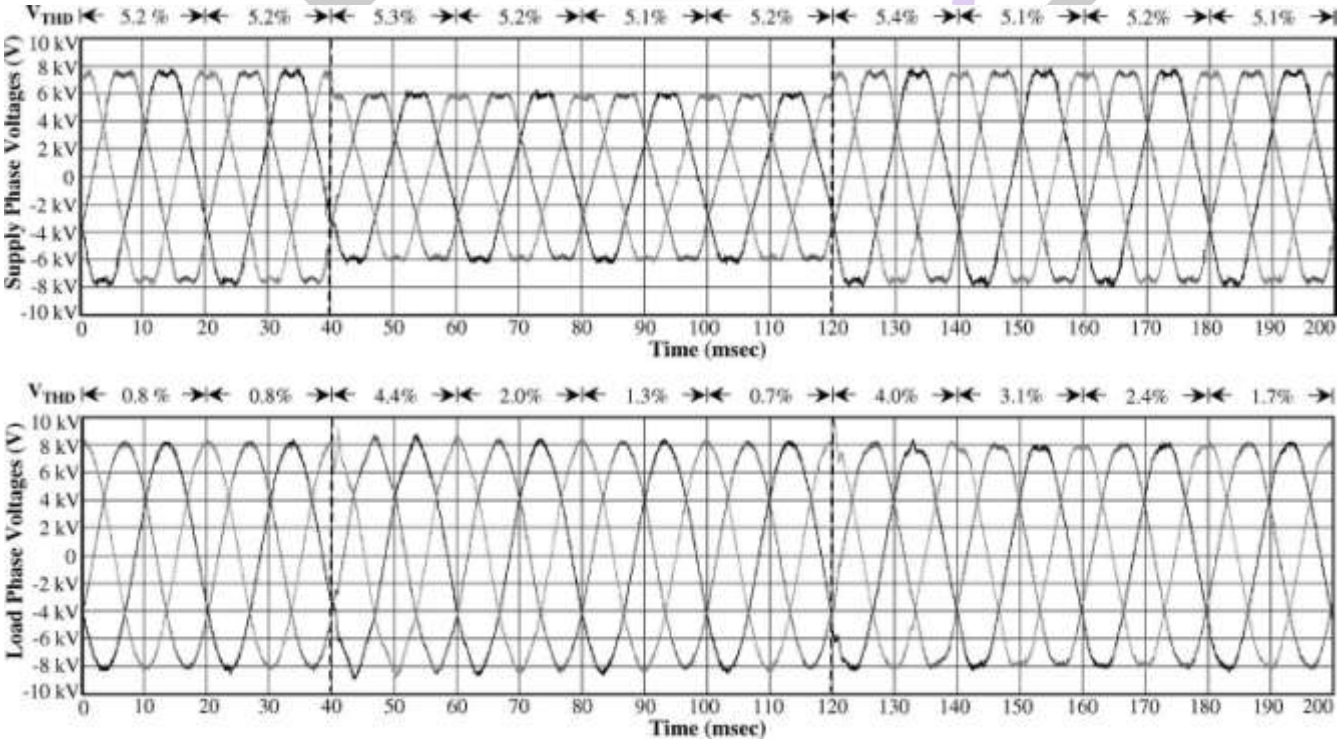


Fig. 11.Experimentally measured compensation of a 0.79 p.u. symmetrical sag with supply voltage harmonics and a linear load (f_c = 1.5 Hz).

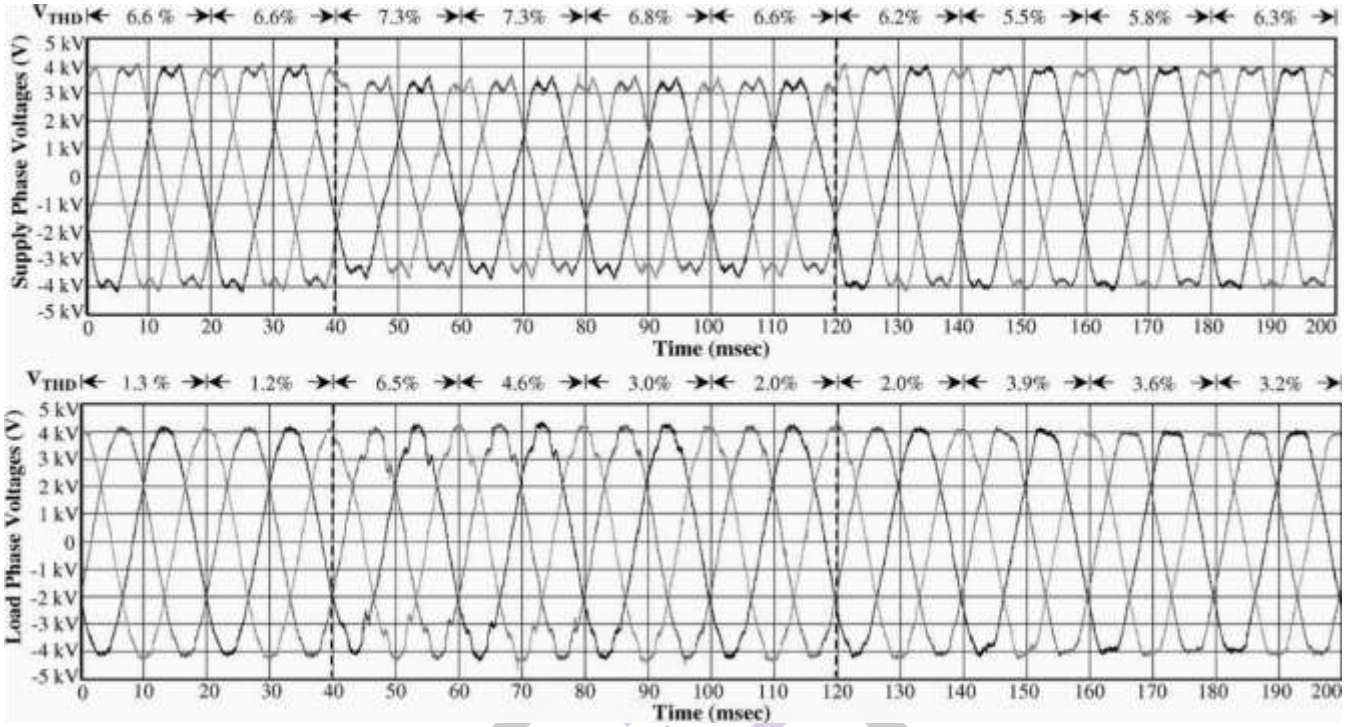


Fig. 12.Experimentally measured compensation of a 0.86-p.u. symmetrical sag with supply voltage harmonics and a nonlinear load (f_c = 0.5 Hz).

Typically, with a switching frequency of 5 kHz or more, the effects of switching harmonics are very minimal. For this system, however, the reference signals are 250 and 350 Hz, rather than the typical 50/60 Hz. Hence, the sidebands are spread much wider around the carrier, wide enough to intrude into the lower frequency harmonic region. Open-loop PWM simulations (using the magnitudes required to compensate for the harmonics in Fig. 8) show harmonics of a little less than 0.1% in the *LC* break point region, confirming this as the extra harmonic source.
Fig. 10 shows a plot for the effect on the load voltage due to disturbances injected at the output of the inverter. In this case, the disturbance is the switching harmonics discussed. (Note that the low-frequency components have an average disturbance rejection less than 0 dB due to the transformer ratio.) This shows that the system is very sensitive to the introduction of disturbances in the

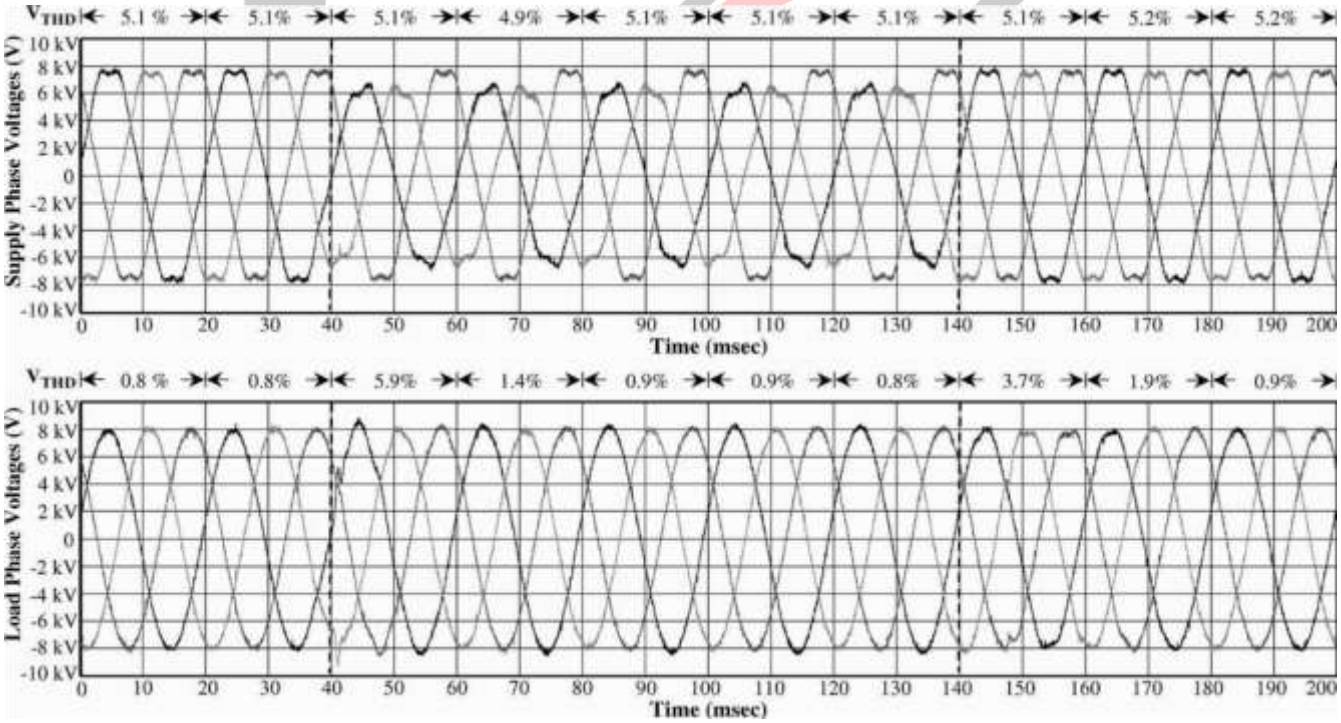


Fig. 13.Experimentally measured compensation of a 0.63 p.u. asymmetrical sag with supply voltage harmonics and a linear load (f_c = 1.5 Hz).

LC filter break point region, which is as expected since this point is directly connected to the *LC* filter input. Furthermore, correlation between this plot and switching harmonics of the magnitude previously discussed, results in a very similar magnitude of introduced harmonics as are seen in Fig. 8(b). While further analysis of this is beyond the scope of this paper, it highlights that for optimum overall performance, such effects as the switching scheme, *LC* filter values, nominal dc-bus voltage, and the switching frequency should be taken into account during the design of the inverter parameters to avoid extra excitation in this region from the inverter. Note that an active damping scheme would also be useful here, although the previously mentioned real power flow constraints limit the use of most conventional schemes for this particular system topology.

The selective harmonic compensation creates an equivalent low-impedance condition at the selected frequencies (i.e., zero magnitude and zero source impedance). However, for these tests, the effect of voltage compensation on the nonlinear load current harmonics was minimal, as expected, since the impedance of the distribution transformer between the DVR and this load is the dominant influence. However, if the harmonic compensated DVR was connected directly to the low-voltage side at the load, then there is a possibility for large increases in current harmonics. This particularly refers to voltage stiff nonlinear loads (such as a diode rectifier with a capacitive dc load used here for the experimental work) where large increases in peak current will occur for very low equivalent impedances at certain harmonics (including the fifth and seventh). Therefore, the medium-voltage installation is seen as a more practical installation point for the proposed scheme.

III. CONCLUSION

This paper has presented a selective voltage harmonic compensation scheme that incorporates voltage harmonic compensation capability into a dynamic voltage restorer (DVR). The scheme uses resonant feedback-based controllers to selectively remove load voltage harmonics, and can be applied to both single- and three-phase systems. The results show that very effective regulation of the selected harmonics can be achieved without affecting the performance of the existing sag compensation controller. Design considerations for the proposed scheme have been discussed, with particular focus throughout on the effect of varying the cut-off frequency of the resonant controller, as well as the effect that various disturbances in the supply voltage and output of the inverter have on the load voltage target.

The work presents experimental results from a 10-kV DVR prototype operating under a range of steady-state and transient conditions containing harmonics in the supply voltage to verify the proposed approach. Both linear and nonlinear loads were tested, as well as combinations of symmetrical and asymmetrical voltage sags.

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