Multilevel Inverter with Reduced Switches

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Abstract —Multilevel inverters have been widely accepted for high-power high-voltage applications Though the multilevel inverters hold attractive features, usage of more switches in the conventional configuration poses a limitation to its wide range application. Therefore, 7-level multilevel inverter topology is introduced using less number of switches and gate trigger circuitry, thereby ensuring the minimum switching losses, reducing size and installation cost. By providing gate trigger signal, AC output voltage is generated.

Keywords—Multilevel DC to AC inverter, PIC Microcontroller, PUC Inverter, Cascaded Inverters

I. INTRODUCTION

Important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses.[1]

The elementary concept of a multilevel converter to achieve higher power is to use a series of power semi conductor switches with several lower Voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating ofthe dc voltage sources to which they are connected Percentage of THD for R, RL, RLC load [2]

A multilevel concept is usually a unique alternative because it is based on low-frequency switching and provides voltage and/or current sharing between the power semiconductors. For low power systems multilevel converters have been competing with high-frequency pulse width-modulation converters in applications where high efficiency is of major importance[7]

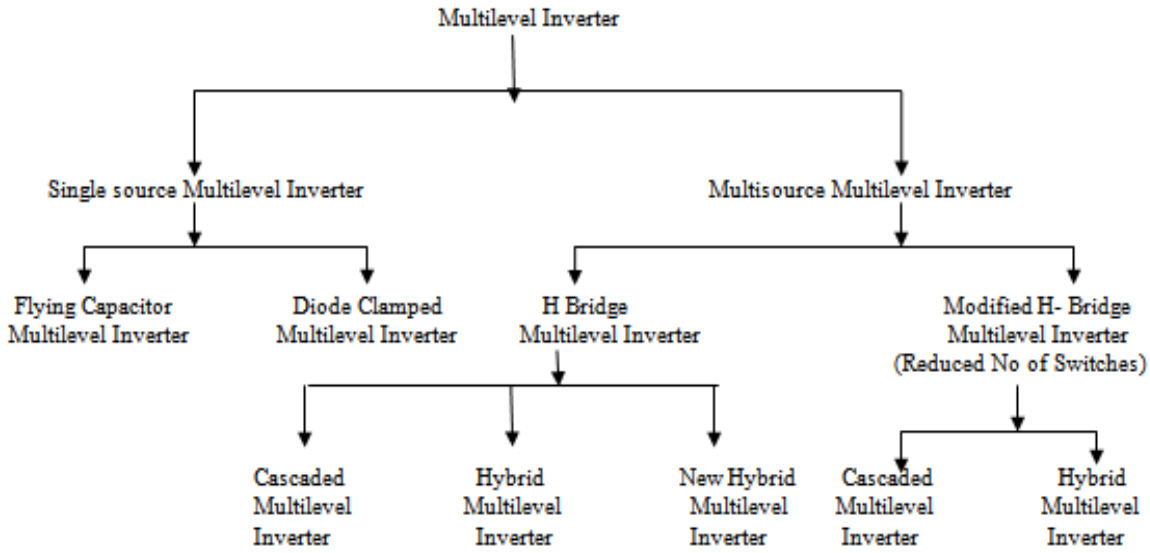
As we know multilevel power conversion has become increasingly popular in recent years due tocompatibility, and can supply high voltage as compared to the value of dc supply. However, as weincrease the levels of output waveform the number of switches in the system also increases and tocontrol these switching devices the number of other components also increases and this lead ustowards complexity as well as higher system cost.

Multilevel inverters have been mainly used in medium or high power system applications, such as static reactive power compensation and adjustable-speed drives. multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application.[9]

Multilevel inverters have received more and more attention because of their capability of high voltage operation, high efficiency and low electromagnetic interference (EMI). The desired output of a multilevel inverter is synthesized by several sources of DC voltages.With an increasing number of DC voltage-sources, the inverter voltage output waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. This results in low switching losses, and because of several DC sources, the switches experience lower voltage stresses.[10]

Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact the development of a novel modified H-bridge single-phase multilevel inverter that has two diode embedded bidirectional switches and a novel pulse width modulated (PWM) technique[11].

Classification of Multilevel Inverter



- **Different topologies of Seven Level Inverter :**

I) New Multilevel Inverter Topology

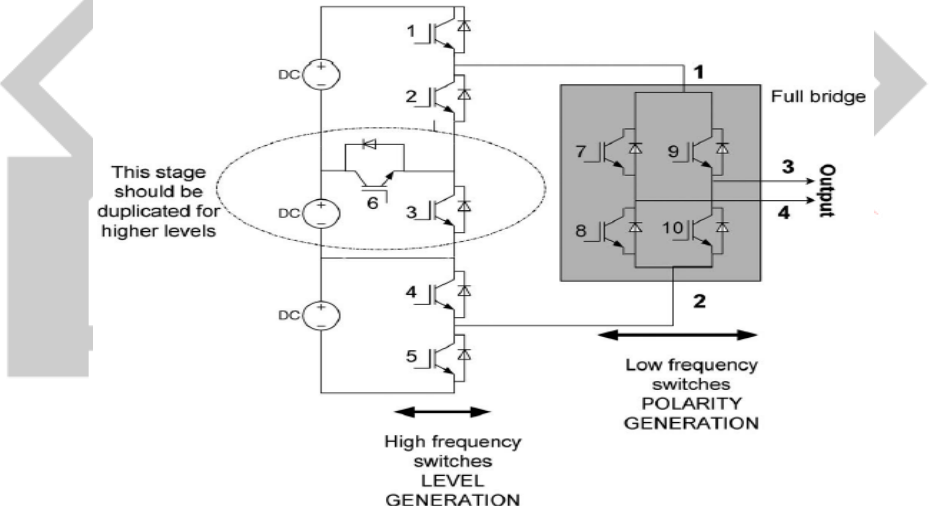


Fig.1.Schematic of a seven-level inverter in single phase

II)PUC INVERTER, MODELLING AND CONTROLLER DESIGN

PUC inverter topology has been first introduced by Al-Haddad et al [30]. It consists of 6 active switches, one isolated DC supply and one DC capacitor as second DC source (or dependent DC source) which is shown .

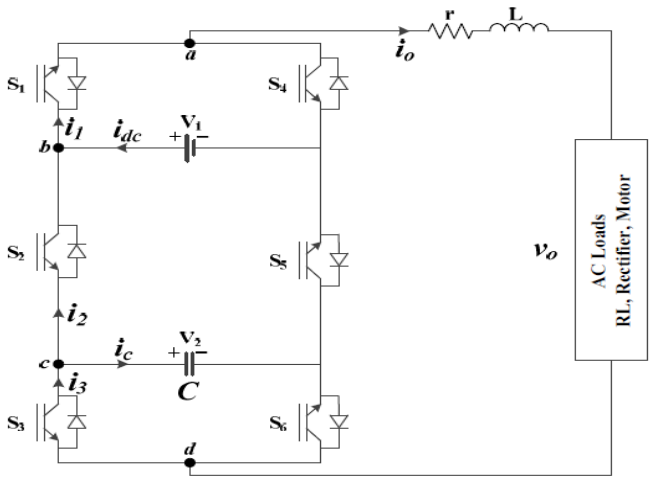


Fig.2. Single-phase PUC inverter

PUC inverter is used which aims at defining a set of pulses for associated switches used in that topology. Based on formulated model, a cascaded nonlinear controller has been designed to fix the capacitor voltage (as dependent DC source) at one third of the reference voltage amplitude and consequently, to generate 7-level voltage waveform at the output with low harmonic contentsand low switching frequency. This paper also deals with real-time implementation and experimental validation of theproposed controller in various conditions including change in load and also in DC source amplitude in stand-alone mode ofoperation. Generating 7-level voltage waveform using only six active switches, one isolated DC source and one capacitorcombined with the proposed low switching frequency voltage controller makes this topology appealing for industries as agood candidate to replace conventional single-phase full bridge inverter in various applications such as renewable energy conversion system, UPS, switch mode power supplies and etc.

III) Single phase diagram of 7-level CHB inverter

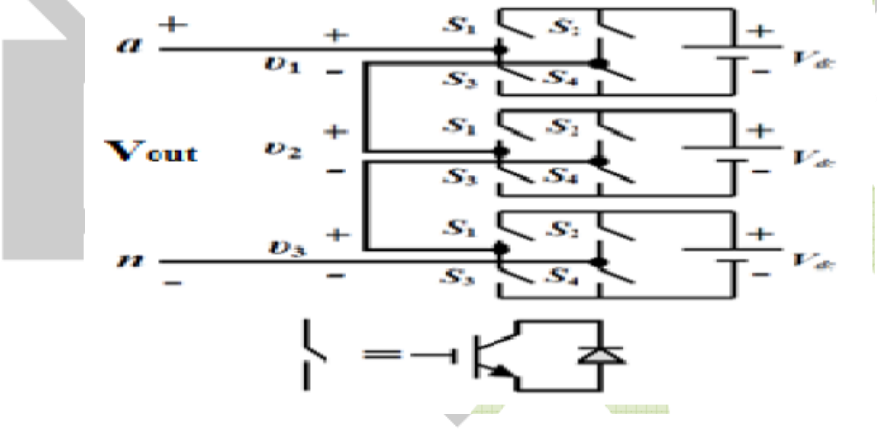


Fig. 3.Single phase diagram of 7-level CHB inverter

The LC filter is also use in the output side to further reduce the THD values. Seven level inverter is utilize as a power converter to inject power generated from pv source to the grid. PV array cell is designed in matlab, and solar is taken as input to the seven level inverter and performance is evaluated.

The traditional two or three levels inverter does not completely eliminate the unwanted harmonicsin the output waveform. Therefore, using the multilevel inverter as an alternative to traditionalPWM inverters is investigated. In this topology the number of phase voltage levels at theconverter terminals is 2N+1, where N is the number of cells or dc link voltages. In this topology,each cell has separate dc link capacitor and the voltage across the capacitor might differ amongthe cells. So, each power circuit needs just one dc voltage source. The number of dc linkcapacitors is proportional to the number of phase voltage levels .Each H-bridge cell may havepositive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltagesand is symmetric with respect to neutral point, so the number of voltage levels is odd.

IV) Single-phase structure of a multilevel cascaded H-bridges inverter

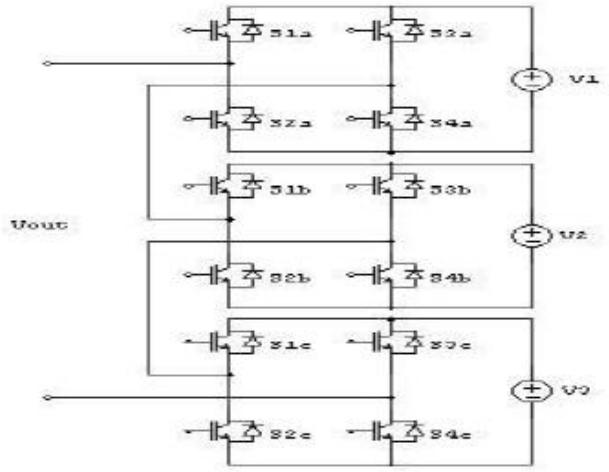


Fig. 4.Single-phase structure of a multilevel cascaded H-bridges inverter

A single-phase structure of an m- level cascaded inverter is illustrated. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and – Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1 , S2 , S3 , and S4 . To obtain +Vdc, switches S1 and S4 are turned on, whereas –Vdc can be obtained by turning on switches S2 and S3. By turning on S1, S2, S3, and S4 the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs as shown in fig2.3. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources

V) Seven level H-Bridge cascaded multilevel inverter (CMLI)

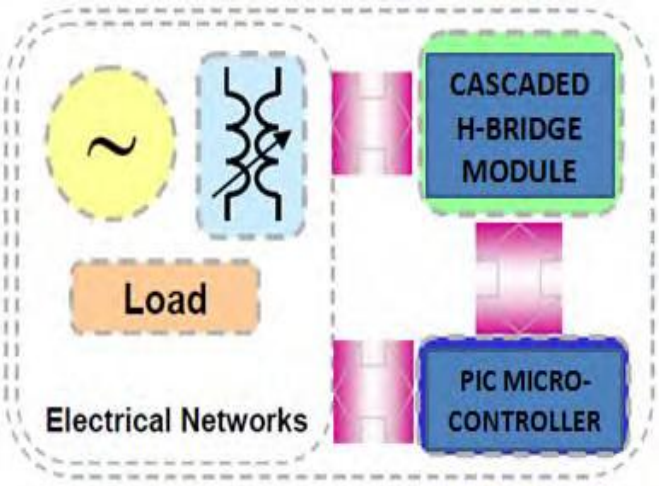


Fig. 5.a) proposed configuration block Diagram

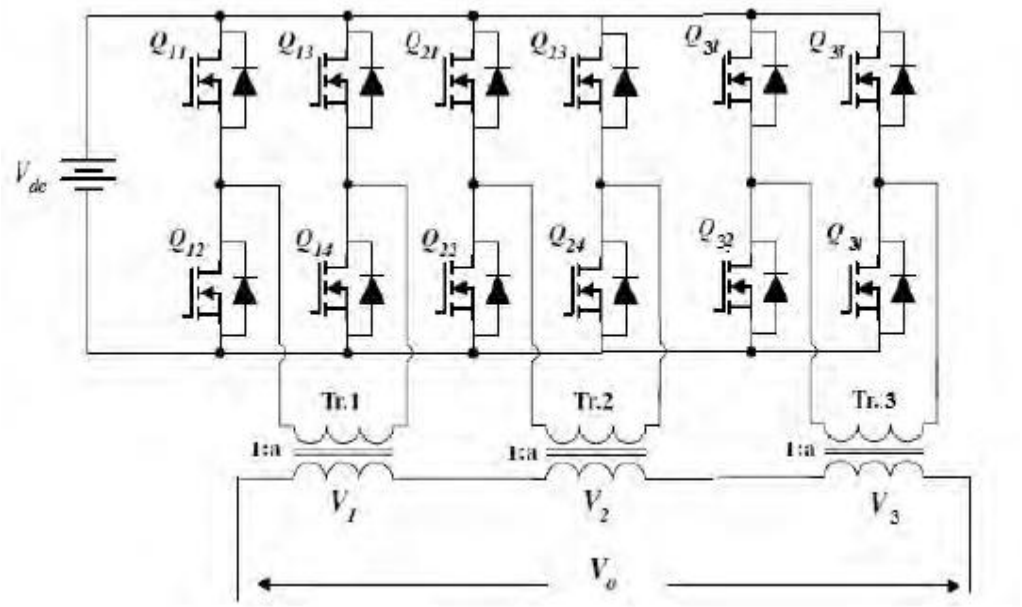


Fig 5.b) Circuit configuration of proposed multilevel inverter

In this single DC source is linked to the H-bridge modules which are connected in parallel along with series connected cascaded transformer in the secondary side. From the operation point of view each and every H-bridge circuit produces 3-level output (+Vdc , 0 , -Vdc) and every transformer secondary is series connected to obtain the required output voltage. In the proposed configuration output voltage depends on transformer turns ratio and input DC voltage. Harmonic components present in the inverter output voltage is reduced by filtering which is provided by the transformer leakage reactance effect The proposed multi-Level Inverter has parallel connected H-Bridge module to synthesise 7-level output. Since each and every H-Bridge module can produce +Vdc, 0, -Vdc then required final voltage (Vo) is obtained by the sum of the output voltage of each cascaded transformers having series connected secondary. In the proposed model employing single DC source the number of output voltage level and number H-Bridge module relation is given by

$$Vo = 2n+1 \quad \text{.....(1)}$$

Where n- number of individual H-Bridge module Staircase switching method employing Multilevel carrier shifted PWM (MSPWM) scheme is utilised as shown in fig 5.Output pulses produced by each H-Bridge module during fundamental switching period having unique lower and upper level as shown in fig.7. Similarly other levels also have different solution which meets their corresponding requirements. Conduction angle (α) is the control factor for each H-Bridge module therefore the proposed circuit shown in fig.2 have control factors α1, α2, α3 respectively.The effective output voltage based on these control factors is given by

$$V_o = V_{dc}\sqrt{\frac{2}{\pi}\left(8\pi - \alpha_1 - 3\alpha_2 - 5\alpha_3\right)} \qquad (2)$$

A suitable solution must be found to diminish the harmonic components present in the output voltage. Harmonic and output voltage fundamental components are analyzed by using fourier series expansion as the ultimate output voltage is an odd function and the Fourier series co-efficient is given as

$$b_n = \frac{4}{\pi}\left[\int_{\alpha_1}^{\alpha_2} V_{dc}\sin(n\theta)d\theta + \int_{\alpha_3}^{\alpha_2} 2V_{dc}\sin(n\theta)d\theta + \int_{\alpha_3}^{\frac{\pi}{2}} 3V_{dc}\sin(n\theta)d\theta\right]$$

$$b_n = \frac{4V_{dc}}{n\pi}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)\right] \qquad (3)$$

The value of control factor is determined from above equation from which we can find higher magnitude of a fundamental component with lower harmonics. The effectual value of fundamental and harmonic component is btained from equation yields

$$V_1 = \frac{4V_{dc}}{\sqrt{2\pi}}[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)] \quad (4)$$

$$V_h = \sqrt{\sum_{n=3,5,7\ldots k}^{\infty} b_n^2} \quad (5)$$

THD is obtained using equation (4) & (5) which is given by

$$THD = \sqrt{\sum_{n=3,5,7\ldots k}^{\infty} V_n^2}$$

$$THD = \sqrt{\left(\frac{\pi(8\pi - \alpha_1 - 3\alpha_2 - 5\alpha_3)}{4(\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3)}\right) - 1)} \quad (6)$$

VI) Topology of Novel Multilevel DC–AC Inverter

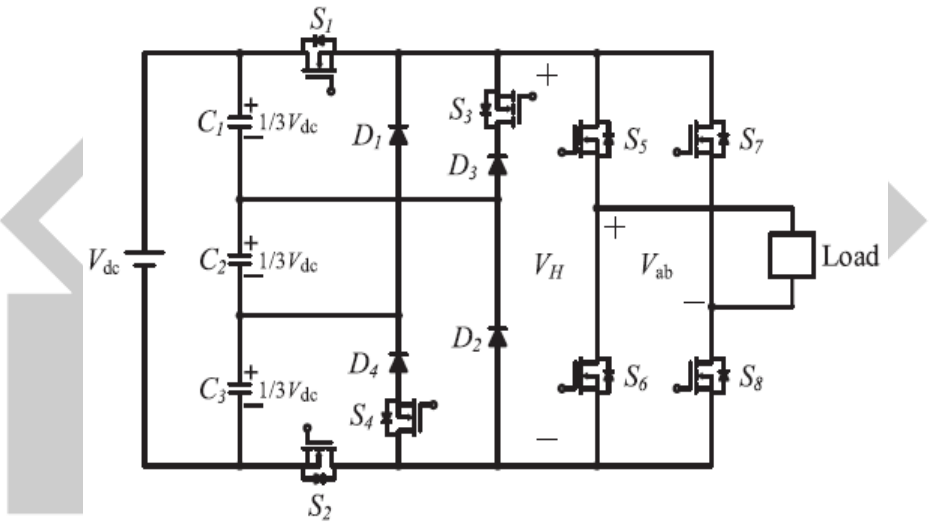


Figure 6: Circuit diagram of proposed seven-level inverter topology.

A.) Circuit Configuration

Fig 2 shows the proposed novel topology used in the seven-level inverter. An input voltage divider is composed of three series capacitors C1, C2, and C3. The divided voltage is transmitted to H-bridge by four MOSFET, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFET. The proposed multilevel inverter generates seven levels AC output voltage with the appropriate gate signals design

B) Operating Principles

The required seven voltage output levels (±1/3Vdc, ±2/3Vdc, ±Vdc, 0) are generated as follows:

1) For voltage generation of Vo = 1/3Vdc, switchS1 is turned on at the positive half cycle while the energy is provided by the capacitor C1 and the voltage across H-bridge is 1/3Vdc. Then the switches S5 and S8are turned on and thus the voltage applied to the load terminals is 1/3Vdc. Fig. 3 shows the current path at this mode

2) For getting level of voltage ofVo = 2/3Vdc, S1 and S4 are turned on while the energy is provided by the capacitor C1 and C2and the voltage across H-bridge is 2/3Vdc,.After that switches S5 and S8are turned on and thus the voltage applied to the load terminals is 2/3Vdc. Fig. 4 shows the current path at this mode

3) For attain voltage level of Vo = Vdc, S1 and S2 are turned on while the energy is provided by the capacitor C1, C2, andC3 and the voltage across H-bridge is Vdc. Thus switches S5 and S8are turned on and thus the voltage applied to the load terminals is Vdc. Fig. 5 shows the current path at this mode

4) For generation of voltage level Vo = -1/3Vdc, S2 is turned on at the negative half cycle while the energy is provided by the capacitor C3 and the voltage across H-bridge is 1/3Vdc.Then the switchesS6 and S7 are turned on and thus the voltage applied to the load terminals is -1/3Vdc. Fig. 6shows the current path at this mode.

5) For next voltage level Vo = -2/3Vdc, S2 and S3 are turned on while the energy is provided by the capacitor C2 and C3and the voltage across H-bridge is 2/3Vdc. After that switchesS6 and S7 are turned on and thus the voltage applied to the load terminals is -2/3Vdc. Fig. 7 shows the current path at this mode.

6) For getting level of voltage Vo = -Vdc, S1 and S2 are turned on while the energy is provided by the capacitor C1, C2, and C3, the voltage across H-bridge is Vdc. Then the switches S6 and S7 are turned on and thus the voltage applied to the load terminals is -Vdc. Fig. 8 shows the current path at this mode.

7) To generate a voltage level Vo = 0, switchesS5 and S7 are turned on and thus the voltage applied to the load terminals is zero. Fig 9shows the current path at this mode

C) Table 1-Switching combinations required to generate the seven-level output voltage waveform

Output voltage Vo	Switching combinations							
	S1	S2	S3	S4	S5	S6	S7	S8
1/3Vdc	ON	OFF	OFF	OFF	ON	OFF	OFF	ON
2/3Vdc	ON	OFF	OFF	ON	ON	OFF	OFF	ON
Vdc	ON	ON	OFF	OFF	ON	OFF	OFF	ON
- 1/3Vdc	OFF	ON	OFF	OFF	OFF	ON	ON	OFF
- 2/3Vdc	OFF	ON	ON	OFF	OFF	ON	ON	OFF
- Vdc	ON	ON	OFF	OFF	OFF	ON	ON	OFF
0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF

CONCLUSION:

As seven level multilevel inverter can be done by different ways as stated. but Multilevel Inverter with Reduced Switches which will requires minimum number of switches with increased stepped output which is near sinusoidal. Due to fewer switches optimized circuit layout and packaging is possible. Compared with conventional inverters it requires less number of components to achieve same number of output levels.

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