DESIGN AND IMPLEMENTATION OF CIRCUIT OPTIMIZATION IN VLSI

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***Abstract*: Digital circuits simplify the operation of transistors and allow devices to be built as switches. Advent of vacuum tube had an enormous impact on the electronics industry but some obstacles such as high power and a hundred anode tension. In the microelectronics industry the invention of transistor consumed few watts. It became the foundation for low-energy appliances. The integration of numerous functions into a single chip and improvement of circuit performance have led to a decrease in the functionality and a growth of power per unit area, which in turn has been complemented by heat removal and cooling system requirements. Throughout the VLSI environment, low power is the biggest issue for them. The environment, power and efficiency are the three most important factors to be optimized nowadays. In the past, efficiency, expense and output were highly significant, with a marginal decrease in strength. With extraordinary battery power development, a complex practical technology such as a computer system, electronic devices, mobile telephones, implantable instruments, digital handheld devices needing low power usage and high speed computing, the need for low power has been increased. High-power machine aggravates other silicone faults through high-temperature activity.**

***Keywords*: Digital circuits, transistors, vacuum tube, VLSI, electronic devices, high-temperature activity**

1. Introduction

In today's world of the electronics industry low power has emerged as a main subject. The area, power consumption and speed are the main concerns for VLSI designers. Dissipation of power has become a significant parameter in the nature of the VLSI module. The increasing speed and complexity of today's designs shows that a wide range of techniques for decreasing VLSI chip energy are increasing considerably. Over the last year, the ICs of 100million transistors have clocked over 1GHz, because strength is taken into consideration over terms of region and distance. The forms of different currents that support the power dissipation have leakage present. The current flows through parasite diodes developed between drain bulk and source mass regions, with a short channel effect induced by a reduction in transistor scaling. The discharge is classified into the dissipation of static power and the dynamic dissipation of power. Static dissipation of the leakage power and the standby force. The power dissipation of the short circuit due to the current is dynamically dissipated.

2. VLSI CIRCUITS

Computers for processors, RAM, control module, etc. use embedded modules. ICs often refer to switching mechanisms, messaging platforms, computing networks, cars, audio instruments, toys and body implants. The technology of the Micro-Electro - Mechanical System (MEMS) facilitates the production of interdisciplinary mechanical equipment on IC, combining small scale mechanical and electronic systems. Sensors and acceleration capability for automotive airbags are, for example, installed on a chip where an accelerometer sense a rapid increase in the car speed and detects an impending crash. These developments made the ICs for common use and one of the greatest accomplishments of mankind.

In these last five decades, the transistor count has grown from a few hundred to more than 20 million. The transistors are five generations. In the last decade in particular, major advances for electronic devices and mobile phones have been noted in the IC industry. This makes it very obvious in the coming decade that several Giga Hertz can be used for chip building with millions of transistors and that millions of mechanical and electrical equipment can be used for Micro Electronic mechanical chip construction. These chips will allow a new age of mobile devices that includes these applications as augmented perception, wearable and implantable computers. It will provide all people with cost-effective, regional point-to - point connectivity. The evolution of IC technology began in the 1960s with the inclusion of very few transistors (SMIS). Millions of transistors combined into one chip are actually being referred to as VLSI (Very Large Scale Integration) chips. Modern ICs were simpler and provided a few flip-flops and gateways. For a single transistor with a simple condenser network, some ICs were more intelligible for performing a logical function."

Over the last ten years, very large interface architecture has been evolving enormously with screen sizes reduced from the micrometer to the nanometer. The rule of Moore notes that every 1.5 years the cumulative transistors on a single integrated circuit increase. The transfer ranges of several hundred transistors per circuit to the several millions of transistors per day per single chip. Only by reducing the feature sizes of the integrated circuit is this significant migration possible. The practical sizes were changed from only a few meters to only a few nanometres. In order to achieve high device efficiency, electronic design automation (EDA), due to the growing difficulty of modern VLSI chip design, plays an significant role. The architectural planning process for VLSI includes partitioning, floor planing, arranging, routing and compacting. The big increase in VLSI circuits will in future depend upon the advancement of resources for physical system automation.

The problem of minimizing these interconnect delay and interconnect power dissipation has been addressed at routing stage. Routing is the process of arranging circuit wires on a layout. In VLSI design, routing consists of determining shortest path between

source to sink positions of all blocks on the layout, such that the wire lengths are minimized and constraints are satisfied. This work proposes the minimized interconnect power dissipation, the minimized interconnect delay, avoidance of the routing path congestion."

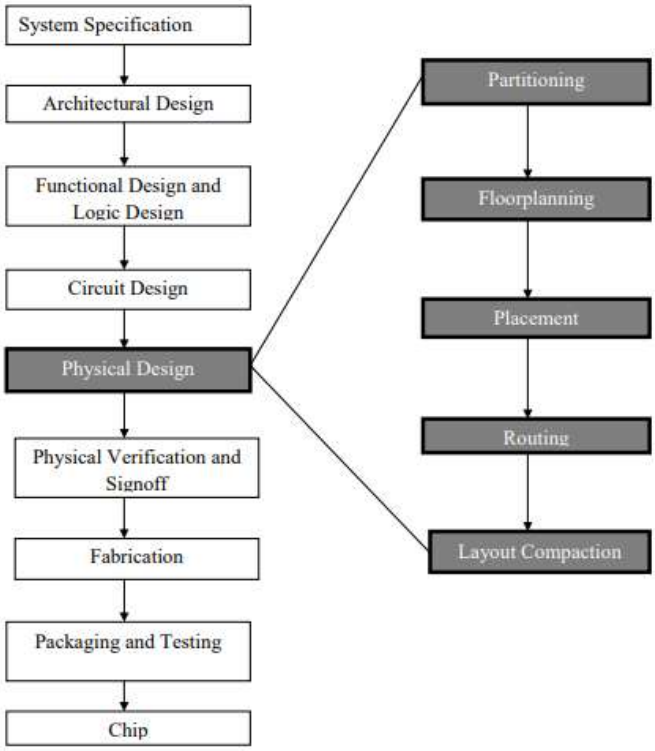


Figure 1.1 Process of VLSI design

3. CMOS Circuits Power Dissipation: Sources

Energy dissipation may be triggered by 4 causes in CMOS optical circuits:

- the dc path between the rail of supply during output transitions, the short circuit current
- Capacitation (switching) current to load and unload condenser loads during logical transitions
- The dc current taken continuously from V dd to field, static or standby current.
- leakage current from diode currents and sub-ground consequences of reverse bias

The equation can therefore be expressed in the full average power dissipation of the CMOS circuits:

$$P_{avg} = P_{switching} + P_{\text{short circuit}} + P_{\text{leakage}} + P_{\text{static}}$$

$P_{switching}$ = switching component of power given by the equation:

$$P_{switching} = \alpha . C_L . V_{dd^2} . f_{clk}$$

Where α is an operation component of node transfer (the total amount of cycles the node change takes one cycle, C L is the load capacitance, Vdd is the voltage of transmission and FCl is the frequency of the device). The main source of power dissipation is dynamic power. The dynamic dissipation of power reduction requires the reduction of one of the equation parameters (2). The criteria are not unique. This must be remembered. The most effective way to reduce dynamic power is to reduce supply voltage, as there is a quadratic power drop. Reducing the transmission voltage thus raises the delay and reduces the circuit output. The clock frequency always needs to be decreased to allow the circuits to work correctly. Reducing capacity is another way of reducing power. For fewer circuitry, simpler devices, less and shorter wires, the power may be minimized but transistor sizes often improve their speed. The third way is to decrease the activity that again depends on the clock frequency and data transition activity. A significant proportion of energy consumption is represented in digital CMOS circuits by dynamic power.

4. Domino Logic Technology Mapping

Technology mapping is an essential step that captures the behavior of the circuits with the help of various gates. In the last chapter, after decomposition we have obtained a static and Domino logic block. Mapping the Domino logic can be done in different ways. In this chapter, we propose a method to map the Domino logic block so that the overall delay is minimum.

We call it the approach of CRDOM. First, with a node mapping algorithm we convert a given unat network to a net list of larger Domino cells. Next, we seek to reorganize the cells in this important route, which reduces the pause further. Finally, None of the literature treated unallowed circuits as their source. The works that took a parameterized map of libraries did not focus on critical path management. There is thus an immediate need for the implementation of a methodology of mapping, in order to attain high efficiency, to incorporate large functionalities in one cell while concurrently fine tune cells. Domino's flexibility in the design of the individual cells leads us to look in this direction. In addition, the critical pathway is rearranged in a way that minimizes further time. Fine tuning of these cells along the critical path is indeed a challenge without increasing the number of their individual transistors.

Methods Proposed

An overview of our proposed approach CRDOM is shown in Figure 3.1. Our approach consists of the following. Given a unate block Cinit which is totally unate in nature. Consider Ldom be the library of various gates that are required to map the initial logic." Raw_Map: An on-the-fly mapping step, represented as Raw_Map which takes the circuit Cinit comprising a set of gates g1, g2, . . . , gn as input and gives CRaw_Map as the resulting circuit which comprise an additional set of gates G1, G2, . . . , Gk, which obey certain width, height constraints. Here, we can represent this as,

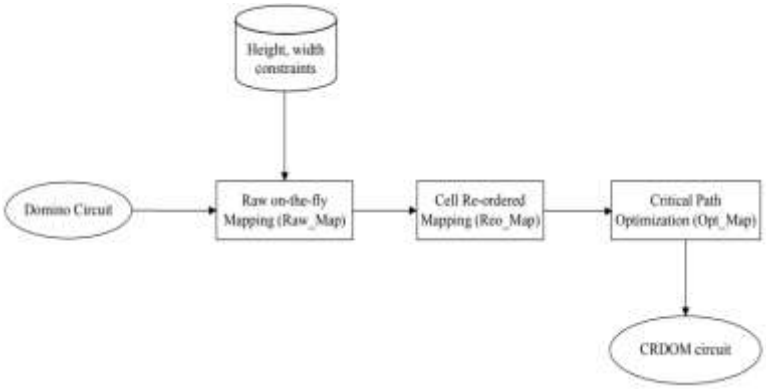


Figure 1: CRDOM approach Overview

$$Raw\_M\ ap\{Cinit(g1, g2, \ldots, gn)\} \rightarrow CRaw\_Map(G1, G2, \ldots, Gk)$$

Opt_Map:"Suppose,$Opt\_Map\{C_{Reo\_Map}(G_1^*, \ldots G_2^*, \ldots . G_m^*)\} \rightarrow C_{Opt\_Map}(G_1^o, G_2^o, \ldots G_m^o)$,
where $(G_1^o, G_2^o, \ldots G_m^o)$ are the final gates present along the critical path of the circuit."
Reo_Map: A reordering step which takes input as an on-the-fly mapped circuit and verifies whether or not, each gate present along the critical path is at its lower bound realization with respect to delay. If not, this step changes the gates with the corresponding functionally similar gates which are lower bound with respect to delay. Here, this is define as $Reo\_Map\{C_{Raw\_Map}(G_1, G_2, \ldots, G_l)\} \rightarrow C_{Reo\_Map}(G_1^*, G_2^*, \ldots . , G_m^*)$, where $(G_1, G_2, \ldots, G_l)$ are gates obtained after Raw_Map step and $(G_1^*, G_2^*, \ldots . , G_m^*)$, are gates obtained after Reo_Map step.

Boolean Logics Decomposition

An initial study showed that pure domino circuit in terms of area, power and delay is not advantageous for a particular logic. It is since, fundamentally monotonous, the Domino logic model achieves stronger results even when the entire process can be done with inverted gates. In other words, to get the benefit of Domino logic style, better if we apply it to unate part only. This necessitates to decompose a logic into optimum unate and binate parts. This chapter addresses how an initial decomposition of a Boolean logic can be obtained and then optimization of the decomposition. In this work, we propose an influence based unate decomposition algorithm which decomposes a given circuit into a set of unate and binate components. Later using an optimization technique we balance these two blocks for the optimum performance of overall circuit. Our objective of optimization is to judiciously mix static and Domino logic styles in the same circuit to gain in terms of power and speed simultaneously.

5. Methods Proposed

Given a Boolean logic, we are to realize a CMOS circuit, combining both static and dynamic CMOS logic styles. In this section, we present our proposed approach to realize static dynamic mixed CMOS circuits. An overview of our approach is shown in Figure 3.1. Our approach can be stated as follows. Suppose, given a circuit Cinit, whose Boolean function is represented by f(X). X is the input vector, where $X = (x_1, x_2, x_3, \ldots \ldots , x_{n-1}, x_n)$. Our approach consists of the following tasks.

Optimium unate decomposition (OUD): An optimization of a given unate-binate set is performed in this step. After the initial unate decomposition, we obtain unate and binate sets. Judicious mapping of unate set using Domino logic style, and the rest using static logic style would result in an optimum performance of the circuit. We try to obtain the optimum combination in this step.

Library based technology mapping (LTM): We use Ldyn, Lstat the dynamic and static gate libraries for mapping the unate and binate sets, respectively. These mapping of the sets by using cell libraries also helps us in estimating the power, area and delay of the circuits so realized. In the following, we describe the above mentioned steps in details.

Initial unate decomposition (IUD): We decompose the Boolean function f(X) = U(X) ∪ B(X), where U(X) is a unate function and B(X) is a binate function. We call this decomposition as initial unate decomposition (IUD). U(X) is meant for realizing the circuit with Domino logic whereas B(X) is for static logic style

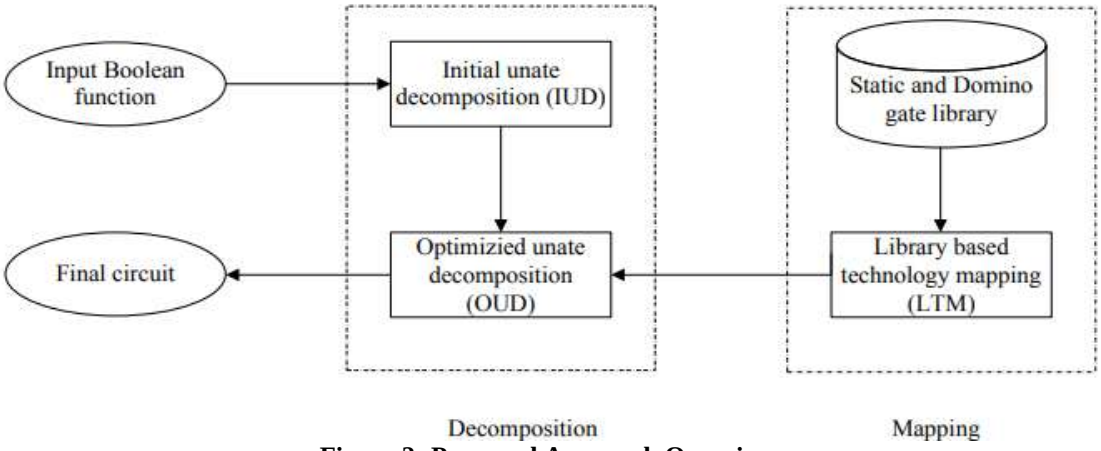


Figure 2: Proposed Approach Overview

6. Decomposition of Initial unate

We recommend an algorithm which takes a totally characterized Boolean function as input and decomposes it into binate and unate parts. This algorithm is termed as IUD. The various steps of IUD algorithm are shown in the form of a flowchart in Figure 4.2

$$f(x) = \bar{x_3}\bar{x_1} + \bar{x_2}\bar{x_1}\bar{x_0} + x_3\bar{x_2}x_1x_0 + x_3x_2x_1\bar{x_0}$$

Where the number of input variables n = 4.

Step 1: In this step, we obtain the onset (OS) states of the Boolean function f(x). For example, the OS of f(x) is {0, 1, 4, 5, 8, 11, 14}. Note that realizing the OS elements is equivalent to realizing the original Boolean function.

Step 2: We construct a POSET for the OS. For the example OS, the POSET is shown in Figure 3.3. This POSET has states with 5 different weights 0, 1, 2, 3, 4. Hence, there are five levels in the POSET (Lemma 1). The elements which belong to the onset are shown using grey ovals and the remaining are in white ovals. The decimal value of the elements is shown adjacent to the ovals.

Low Power: Clock Gating

In this chapter we concentrate on reducing the power dissipation by clock gating of the domino blocks. Time gating is an important method to avoid duplicate reasoning from being loaded and unloaded in a certain device. Many studies on the implementation of clock gating have been published in recent literature. Yet most of them just worked on serial circuits. Since the outputs of a composite block depend entirely on its origin, sequential and hybrid circuits cannot use the same technique to clock gating at the same time. In fact, all of these plays were planned to reduce the routing time of the clock, to resolve the slew constraints, etc. In addition, it is important to investigate a way of rising redundant gate changes in dominino circuits. Constantly flipping domino blocks for any clock pulse rise is a power-hungry operation that can be alleviated by using a gating strategy as a time-gating solution. Around the same time it appears to be a daunting challenge to reduce unnecessary movements and retain a regulation of the reasoning overhead.

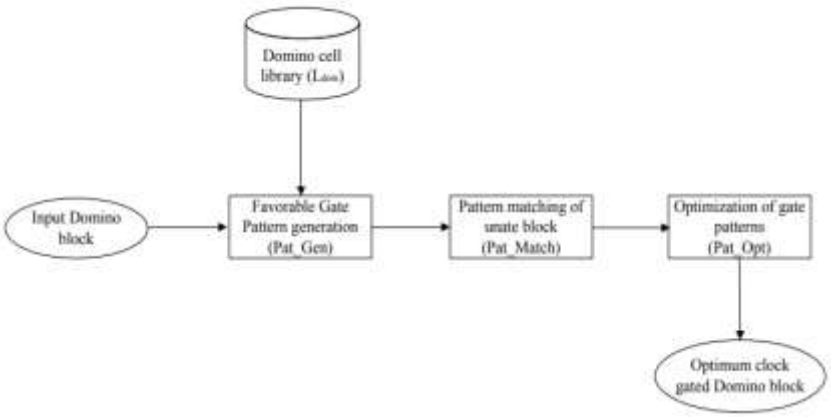
We deliver a clock matching program based on the Domino circuit pattern recognition technology. We first create a collection of gate patterns from the Domino cell library that can be targeted. that is to say, patterns, which can result in positive clock gates savings. We instead use an algorithm based on the index subsection graph that maps the FGPs that have obtained to a given circuit's Domino row. Within this Section, you can consider how we deal with problems in the detection of FGPs and the maping of the fGP to the circuit."

7. Methods Proposed

An overview of our proposed methodology is presented in Figure 5.1. Our overall approach consist of the following operations." Suppose, given a circuit C_{init} which is completely unate in nature. Let L_{dom} be the Domino cell library used for mapping. We brief the different tasks in our approach as follows.

Pattern generation (Pat_Gen): A pattern generation step, denoted as Pat_Gen, which tries to generate a set of favorable gate patterns (FGPs) from a given L_{dom} such that each individual gate pattern (p_i) is associated with power savings (P_{sav}) area penalty (A_{pen}) with it, simultaneously satisfying the constraint $(P_{sav} > 0)$. We can define this as $Pat\_Gen\{L_{dom}\} \rightarrow \{p_1, p_2, \dots, p_k\}$ $where$ $\{p_1, p_2, .., p_k\}$ are in the set of FGPs.

Pattern matching (Pat_Match): A subgraph matching operation, where the individual FGPs (subgraphs) are matched to the given circuit (C_{init}) using an index based subgraph matching algorithm (ISMA). We can formalize as, $Pat\_match\{C_{init}, p_i\} \rightarrow \{P^i_{sav}, A^i_{pen}\}$ where p_i i is a considered FGP, P^i_{sav}, A^i_{pen} are the obtained power savings and area penalty after matching is performed.



Overview of optimum clock gating of Domino circuit

Pattern optimization (Pat_Opt): Pat_Opt is the optimization operator, $p_1, p_2, .., p_l$ are the l optimum patterns and $\{P_{sav}^{opt}, A_{pen}^{opt}\}$ are the resulting power savings and area penalty after optimization. In other words, P at_Opt $\{U_{opt}, p_1, p_2, .., p_k\} \rightarrow \{p_1, p_2, .., p_l, P_{sav}^{opt}, A_{pen}^{opt}\}$ is an optimum pattern matching with respect to some objectives.

This thesis suggests a pattern recognition clock gating for static mixed domino logic circuits. Additional logic and routing are required to enforce clock gating for complex circuits. If it is not taken into account, this improves the total circuit's region and power dissipation. This paper suggests an efficient gated circuit with a clock. Such a circuit is ideal both in terms of power and distance. By comparison to the non-clock gated circuits, the new gating solution still provides significant power savings. Clock gating is comparable to other clock gate strategies mentioned elsewhere for pattern recognition. Our suggested clock gating solution can be considered to be particularly suitable for low-performance applications such as hand-held devices, rechargeable devices, etc."

8. Conclusion and Future work

In this thesis, we have proposed an approach to synthesize VLSI circuits using mixed static Domino CMOS logic style. The main objective of our research is to synthesize Boolean circuits targeting low power dissipation and offering high performance. In this Chapter, we present the various contributions of this paper. The cell re-ordering based mapping approach presented in this offered a significant delay advantage compared to the standard Domino mapping technique. Also, the area penalty imposed while cell re-ordering is kept as minimal as possible. Especially, this approach makes the design suitable for high performance applications. The proposed decomposition based approach presented, yields lower transistor count competed to static CMOS logic style. A Mixed CMOS circuits are comparable with only dynamic and only static realizations according to works stated elsewhere. Also, We may conclude that mixed CMOS circuit is perfect for high speed and low power applications such as handheld digital gadgets, mobiles etc. Significant power savings were recorded by using the pattern recognition based clock gating approach, presented. The clock signal, which is highly active in the Domino block is thoroughly dealt with in this chapter. This made the overall design comparable to other low power approaches reported in the literature. This encourages the design to be used in various application of handheld gadgets. Unate Decomposition: The first contribution of this thesis is an approach to decompose a Boolean logic suitable for realization of a mixed static Domino circuit. In order to realize a circuit by using Domino logic, it must be fully unate. Though, complete unate circuit is physically impractical. So, this work proposes an methodology to get an optimum unate binate circuits. Such a circuits can be synthesized reducing power, area and delay. Given a circuit, we perform an initial unate decomposition (IUD) which we optimize to reduce power dissipation and delay. The third innovation from our research is a pattern identification-based clock gating for domino logic circuits. Additional logic and routing are required to enforce clock gating for complex circuits. Enhanced field and dissipation of control of the whole circuit if due action is not taken. This paper suggests an efficient gated circuit with a clock. Such a device is suitable for power dissipation as well as field retribution. Provided the domino-plot the favorable gate patterns are first generated and the circuit is traced using favorable gate patterns from the domino cell library. We then consider the right conditions, which will achieve full power savings with a minimal surface penalty."

9. Future Scope

The decomposition methods can be further generalized for incompletely specified Boolean functions. This work however leaves a number of issues opens and problems to address giving a scope for further extension of this research. The raw mapping approach considered the gates to be of "and", "or" natures only. Further functionalities can be considered in the initial mapped circuit and new set of rules can be derived accordingly for combination operations. Concepts like average case delay in terms of incompletely defined Boolean functions and usage of logical effort in estimating the delay can also be employed. Also, various other approaches for multi objective optimization and choosing of the best candidate from the Pareto optimal front can be explored. The clock gating logic is optimized using our proposed approach in terms of switching power and area. However, the gating logic significantly affects the delay of the circuit. Hence performance parameter can also be included in the analysis. Our cell mapping strategies attempted to optimize area and delay in the proposed technique. We can also study the effects on parameters like power delay product and energy delay product so that circuits with low power and high performance can be designed. Further, precise models based on deterministic clock gating can be explored which will help in pipelining of circuits.

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