T-Type five level DCMI with Double voltage boosting gain

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***Abstract*: The switched-capacitor-based cascaded multilevel inverters (CMI) have been emerging due to their voltage boosting capability. Unfortunately, they suffer from impulse charging current and nonuniform operation. This article presents a topology termed as dual-T-type five-level CMI to resolve these problems without compromising the desirable voltage boosting characteristic. The main idea is to integrate a half bridge and an inductor to soft charge a capacitor that is connected in series with the dc source. The capacitor enables the voltage gain boosted to two, while the control of eight power switches that constitutes a dual-T structureenables five voltage levels generation. In addition, uniform opera-tion is achieved for cascaded extensions. The operating principle of the proposed topology is analyzed and elaborated. For validation, simulation, and experimental results of a prototype are presented.**

***Index Terms*: Cascaded multilevel inverter, dual-T-type topology, soft charging, switched-capacitor, voltage boosting.**

INTRODUCTION

IN THE last decades, multilevel inverters have been exten-sively researched in view of the continuous development of power devices and the fast growing need for emerging appli-cations such as microgrid. The conventional topologies, i.e.,neutral-point-clamped inverter, flying capacitor inverter, andcascaded H-bridge (CHB) inverter have been proven as ma-ture solutions for industrial applications [1]–[3]. However, thisdoes not hinder continuous research effort in contributing newpromising topologies to offer wider possibilities in multilevel inverter technology [4], [5].

Being one of the most well-established multilevel inverters that has been successfully commercialized, CHB inverter stands out due to its attractive modularity feature. Significant interest has been garnered in the development of alternative modules inplace of H-bridge for improved performance.

To date, various types of cascaded multilevel inverters (CMI) have been proposed in literature. Most of them are based on theconcept of switched dc source [6], where each of its isolated dcsource is controlled by a half bridge to generate unipolar voltage levels across the dc link [7]. Bipolar output voltage is achievedby controlling an H-bridge connected across the dc link. This topology is therefore termed as multilevel dc-link inverter. In asimilar topology in [8], a T-type inverter has been proposed asa replacement for the H-bridge.

In the recent works, considerable attention has been focus ondeveloping cascaded modules by utilizing T-type inverter. An E-type module that combines a T-type inverter, a half bridge, and four additional power switches is presented in [9]. With four asymmetrical dc sources, 13 voltage levels can be gen- erated. A slight modification in [10] can further increase the number of levels to 17 by replacing the half bridge in [9] with aT-type inverter to constitute a two back-to-back T-type invertersstructure. Despite not being mentioned in the literature, it is found that the ratio of asymmetrical dc sources is extended from $2V_{dc}$:V_{dc} to $3V_{dc}$:V_{dc}, which aggravates the power balancing issue. Similar topologies based on back-to-back T-type inverters are also presented in [11] and [12]. The module in [11] can be extended by enclosing more T-type inverters. Alternatively, [12] proposes to extend the module to a switch-ladder structure by connecting more dc sources in series. Optimal design of this topology has validated its lowest power switch count comparedto other cascaded modules. While the freewheeling current during dead-time commutation is not taken into account in the design, this topology is suffering from voltage spikes during transition between voltage levels [13].All the aforementioned modules require the same numberof dc sources as that in CHB due to their limited voltage gain. To address this problem, switched-capacitor (SC) based CMI (SC-CMI) are established [14]–[20]. Self-voltage balancing and voltage boosting are two distinctive benefits of SC-CMI. The former is achieved by charging the SCs in parallel with thedc source, while the latter is achieved by discharging the SCs in series with the dc source. However, these advantages come at the expense of the impulse charging current issue, hindering the implementation of this topology in practical applications. Inaddition, nonuniform operation of SC-CMIs is also a challengethat does not fulfill the modularity characteristic of CMI.

This article proposes a novel CMI topology that resolvedthe impulse current and nonuniform operation problems of SC-CMIs while retaining the merits of self-balancing and voltage boosting. The rest of this article is organized as follows.Section II evaluates the problems of SC-CMIs. Section III presents the proposed topology with its analysis and extensions. Section IV discusses the simulation results. Section V presentsthe experimental results of a prototype. Finally, Section VI draws the conclusion.

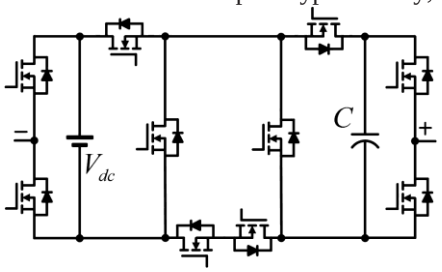


Fig. 1. Five-level switched-capacitor-based cascaded multilevel inverter

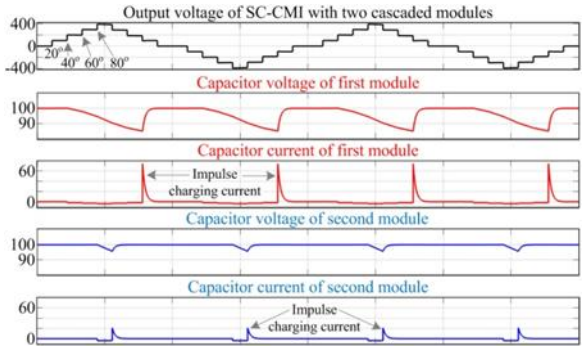


Fig. 2. Simulation results of SC-CMI in Fig. 1 with two cascaded modules

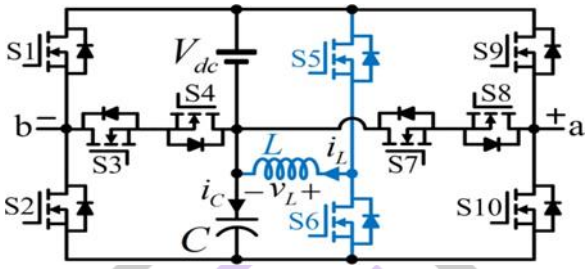


Fig. 3. Proposed DTT-5L-CMI.

PROBLEMS OF SWITCHED-CAPACITOR-BASEDCASCADED MULTILEVEL INVERTER

A five-level topology, depicted in Fig. 1, is considered todemonstrate two principal problems faced by a typical SC-CMI. It is a single-stage topology with one SC that is charged to V_{dc} by connecting it in parallel with the dc source during 0, V_{dc} andV_{dc} levels. Two additional voltage levels are made possible by discharging the SC in series with the dc source. This generates atotal of five voltage levels with the attainable maximum voltagelevel twice of the dc source voltage, thus indicating a voltage gain of two. Fig. 2 shows the corresponding simulation results of the five-level SC-CMI when a dc source voltage of 100 V and power MOSFETs with ON-resistance of 0.1 Ω are considered. With twocascaded modules (n = 2), it is noted that there are nine apparentsymmetrical voltage levels in between 400 and 400 V. The voltage and current of the capacitor in each module, however, reveal the following problems.

A. Impulse Charging Current

The SC is charged to V_{dc} by connecting it in parallel withdc source. The difference between V_{dc} and the SC voltage inevitably leads to the existence of impulse current, which reduces the reliability of the electrolytic capacitor as well as themultilevel inverter. Besides, the use of oversized power MOSFETs with extremely high current rating are mandatory to accommo-date the impulse current. Note that the magnitude of the impulse current is determined by the ratio of capacitor voltage ripple tothe ON resistance of conducting power MOSFETs in charging path.

B. Non uniform Operation

Typically, the charging of SC takes place prior to its discharg- ing process, as illustrated in Fig. 2. Considering the case of unity power factor load in Fig. 2, greater voltage levels are generated in the vicinity of the peak load current (i.e., around 90° and 270° of output voltage) when the SC is discharged. In this instance, exceptionally high-voltage ripples are anticipated. Note that theripple magnitude of the first module is higher than that in the second module due to their different discharging periods. Itis clearly seen that the discharging period for capacitor in the first module is longer than that in the second module, with the former discharges over a span of 100° (40°–140° and 220°–320°)while the latter discharges over a span of only 20° (80°–100° and 260°–280°). Another observation worth emphasized is the different impulse current magnitudes in both modules, which are attributed to the different voltage ripple as mentioned earlier.

It is now clarified that the SC-CMI sacrifices the modularityproperty of CMI as components with different ratings are needed in each module. The shortcoming will be further aggravated ifhigher number of cascaded modules are taken into consideration. This is because the discharging period of the SC between the first module and the last module is elongated. To unify the charging and discharging periods of SC-CMI modules, some special switching strategies are required.

PROPOSED DUAL-T-TYPE FIVE-LEVEL CASCADEDMULTILEVEL INVERTER

The topology of the proposed dual-T-type five-level CMI (DTT-5L-CMI) is depicted in Fig. 3. Voltage boosting is achieved by connecting a capacitor C in series with the input dc source. To prevent the impulse charging current as in the case of SC-CMI, an inductor L that is controlled by a half bridge (S5and S6) is integrated in the topology to achieve soft charging. The rest of the switches constitute two T-type inverters for ac voltage generation.

A. Steady-State Analysis

The switching states of the proposed DTT-5L-CMI are ana-lyzed and summarized in Fig. 4. With capacitor C charged to V_{dc},the maximum voltage level is $2V_{dc}$. Five symmetrical voltage levels are generated in between $2V_{dc}$ and $2V_{dc}$.
Some switches are turned ON despite they are not conductingload current so as to provide a commutation path for the inductive load current during dead time. Taking state [0] as an example, S3 and S8 are two nonconducting switches that are turned ON tocater for the dead-time commutation. Considering the case when there is a voltage level transition from 0 V to V_{dc}, both S7 and S10 are OFF to prevent short circuit across capacitor C. Assuming an inductive load with S8 is ON, the negative load current can freewheel through S8 as well as the antiparallel diode of S7. The load voltage will eventually clamped to V_{dc} during dead time, ensuring smooth transition from 0 V to V_{dc}. On the other hand, if S8 is OFF, the negative load current is forced to flow through the antiparallel diode of S9. A voltage spike of $2V_{dc}$ will be generated during dead time, which is highly undesirable. It is therefore important for all the switching states to be designwith careful consideration to avoid voltage spike during switchtransitions.
For achieving soft charging of capacitor C, S5 and S6 are controlled complementary with a constant duty cycle of 0.5. Energy is stored temporarily into inductor L by turning ON S5 before it is discharged to capacitor C when S6 is switched ON. To reduce cost, S6 can be replaced with a diode. However, active power MOSFET is recommended in view of its bidirectional power flow capability. The switching states in Fig. 4 shows that switches S1, S2, S5,S6, S9, and S10 each blocks a maximum voltage of $2V_{dc}$, whilevoltage stress on the remaining switches are restricted to V_{dc}. On the other hand, the current conduction path analyzed in Fig. 4 depicts that the current stress on S5 and S6 are determined by the inductor current, while that on the remaining switches are equal to load current.

Fig. 4(f) shows that inductor L is used to store energy for thefirst half switching period prior to discharging its energy to ca-pacitor for the remaining period. During steady-state operation,the average voltage of inductor L is zero. Therefore, the averagecapacitor voltage V_C is equal to the dc source voltage

$$V_C = V_{dc}. \quad (1)$$

As inductor L is operated with a constant duty cycle of 0.5, the average power flowing into capacitor C is

$$P_{C,in} = 0.5 I_L V_{dc} \quad (2)$$

where I_L represents the average inductor current. To deter- mine the average power flowing out of the capacitor, the load component of capacitor current $i_{C,Load}$, depicted in Fig. 5, isconsidered. Taking the average of the half-wave rectified current waveform, the average current supplied by the capacitor to theload is $2MV_{max}/\pi R_{Load}$, where M indicates the modulation index, V_{max} indicates the maximum voltage level ($2V_{dc}$).

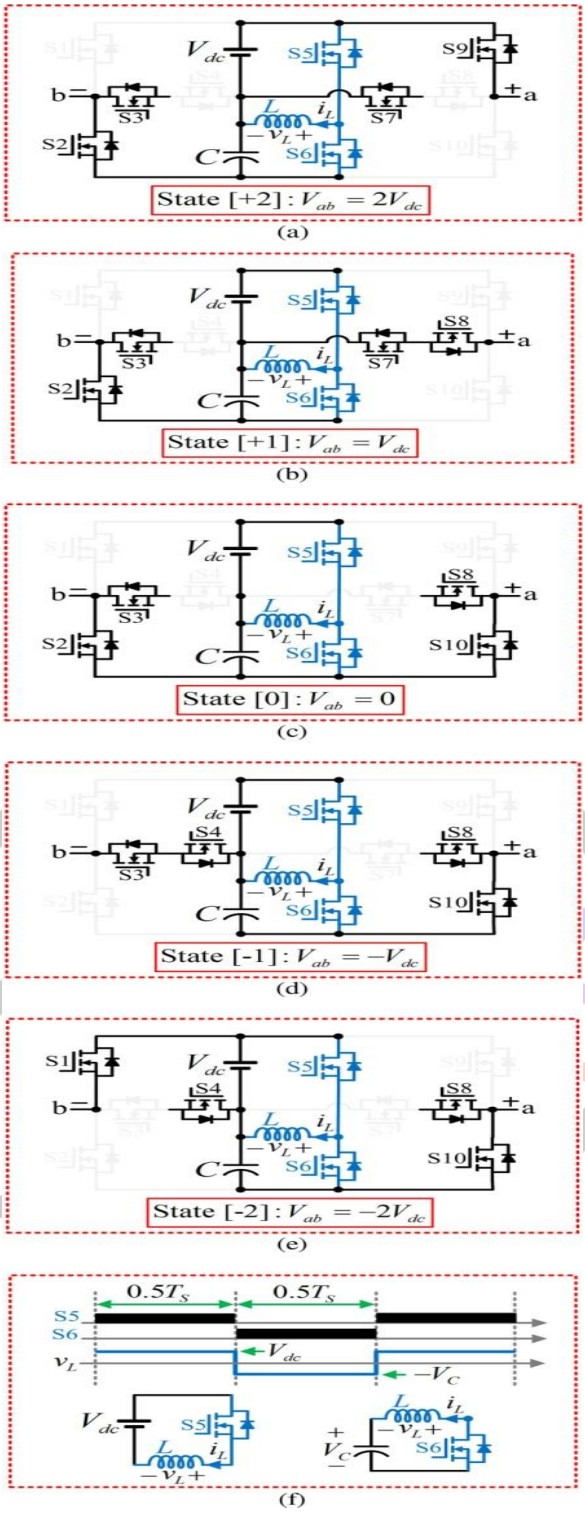


Fig. 4. Switching states of the proposed DTT-5L-CMI: (a) state [+2], (b) state [+1], (c) state [0], (d) state [1], (e) state [2], and (f) soft charging of *C*.

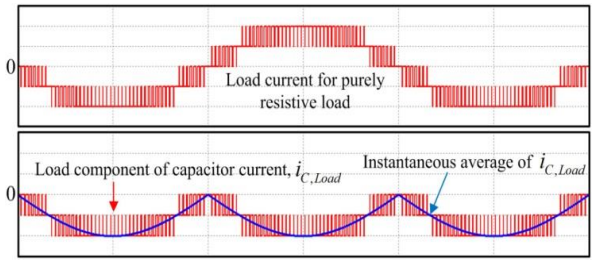


Fig. 5. Load component of capacitor current.

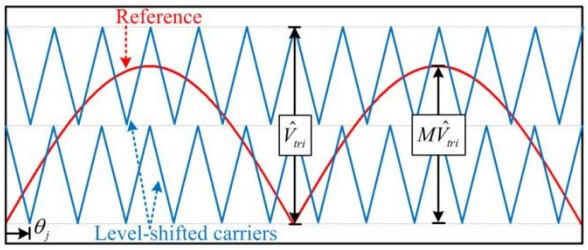


Fig. 6. Modulation scheme for each module.

Comparison with Other Topologies

The SC-CMI has recently arisen as an emerging topology where various configurations are reported in literatures. How- ever, the current spike issue induced from capacitor charging process is rarely discussed. In [21], an inductor inserted in between dc source and SC is used to charge the capacitor withoutcurrent spike. The switching states are designed to synthesize astaircase ac voltage with precomputed duty cycle and switchingangle. Unfortunately, the inductor has to be controlled at fre- quency of only double of that in output voltage, making it not appropriate for power frequency (50/60 Hz) applications. Highoutput frequency of 25 kHz is implemented in [21].

Alternatively, a new SC topology based on CHBs together with a charging circuit consists of an inductor, one diode for each H-bridge, and a switch is proposed in [22]. The capacitor is charged from dc source through a series inductor with antiparal- lel diode to cater for current spike issue. Utilization of antiparal- lel diode is dedicated to prevent the capacitor from overcharging and voltage spike occurrence. It provides a freewheeling current path after the capacitor voltage reaches the dc source voltage. This also signifies that the inductor current freewheels throughthe diode and dissipates power. Special consideration has also been made to avoid continuous increase in inductor current. Discontinuous inductor current is achieved by dissipating the in- ductor energy during freewheeling mode so that the current fallsto zero before the commencement of the next charging cycle.

However, it is worth to emphasize that there is a compromisebetween the inductor size and capacitor charging speed, despitenot deeply discussed. The design/derivation of the inductor value and the corresponding capacitor charging current arenot presented. Small inductance value is usually consideredin this topology owing to the short capacitor charging period. In this instance, the impulse charging current might not be effectively eradicated, as evidenced by the visible impulse current in the presented experimental results [22]. Additionally,the level-shifted sinusoidal pulse width modulation (SPWM) that is deemed to be the most suitable switching technique for this topology results in the undesirable nonuniform operation among H-bridges. Some experimental evidences from [22] clearly demonstrate uneven capacitor voltage waveform with different ripple magnitude, charging period, and discharging period. It should be emphasized that other switching techniquesare less appropriate in this topology due to the restricted capacitor charging pattern, as mentioned in [22].

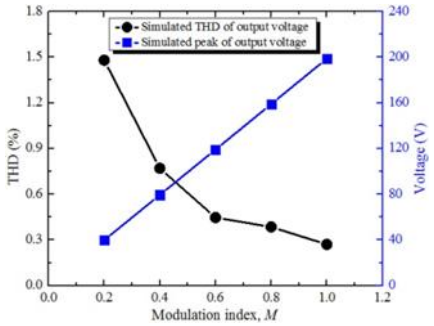
TABLE I
COMPARISON BETWEEN THE PROPOSED DTT-5L-CMI AND OTHER FIVE-LEVEL SC-CMI TOPOLOGIES

	(a)	(b)	(c)	(d)	(e)	(f)
[15]	6	1	1	0	no	no
[22]	9	3	2	1	partially	no
[23]	7	4	2	0	no	no
[24]	13	0	2	0	no	no
Proposed DTT-5L-CMI	10	0	1	1	yes	yes

The proposed DTT-5L-CMI resolved the current spike issueswithout compromising the uniform operation of the CMI. For clarity, a comparison of the proposed DTT-5L-CMI and some recently presented five-level SC-CMI topologies is summarized in Table I. At first glance, the proposed topology requires a moderate number of components count among all. However,in the practical implementation for SC-CMI topologies in [15],

[23] and [24], it is always essential to precharge their SCs to the steady-state voltage prior to turning on the inverter sys- tem. In this regard, short circuit across the dc source can be prevented. However, additional switches in precharging circuitare not considered in these references, and therefore they havehigher switch implementation requirement. The proposed topol- ogy eliminates the need of precharging circuit and it can be conveniently employed for practical applications. Besides, it exhibits a significant advantage over other SC-CMI topologiesby ensuring continuous charging of capacitor from dc source, while simultaneously supplying the loads.

The proposed DTT-5L-CMI resolves the current spike issueof all the contemporary five-level SC-CMIs with improved reliability. With only two additional switches, the voltage gainis enhanced to double as compared to a conventional five-levelCHB. In addition, the number of dc sources is also reducedby half. This indicates that half of the converters required for dcvoltage generation as in a CHB can be eliminated in the proposedtopology. While the voltage boosting characteristic of the pro-posed topology enables single-stage dc–ac power conversion, the dc–dc boost converter can be omitted for improved systemefficiency and reliability, which renders it particularly suitablefor renewable energy systems with low input voltage.



SIMULATION RESULTS

Simulations were conducted to study the feasibility of the proposed topology. Two cascaded modules (n = 2) with dc sources voltage of 100 V each are considered. The simulation results are depicted in Fig. 7. Each module is generating five symmetrical voltage levels between 200 and 200 V. Their maximum voltage level is twice of the dc source voltage, thus validating a voltage gain of two. A total of nine distinct voltagelevels are generated and the maximum voltage level is extendedto 400 V

Individual module is also investigated in this simulation. Observations shows that the capacitor voltage, capacitor current, and inductor current captured for both modules are similar. This implies that the operations for both modules are uniform and the modularity feature of cascaded inverter structure is retained. It is also demonstrated in Fig. 7 that the capacitor charging current is determined by the inductor current. This is because the capacitor in each module is charged through its respective inductor. In this regard, soft switching is achieved and no impulse current isobserved in the plotted capacitor current waveforms.

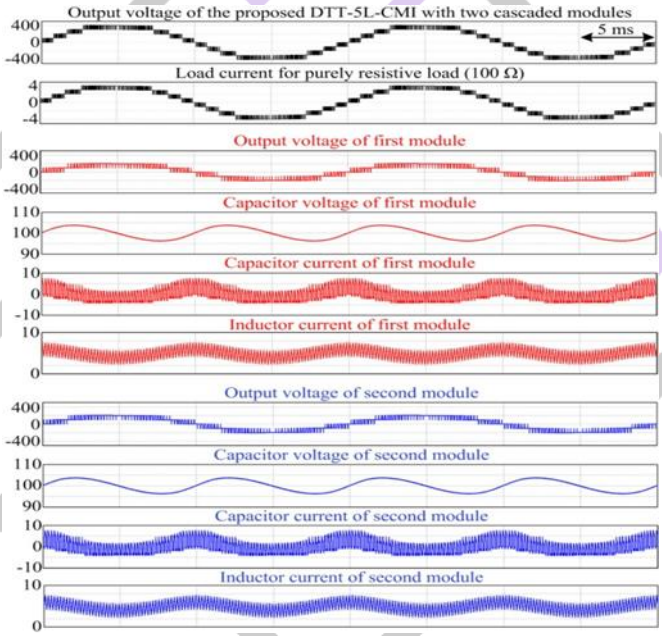


Fig. 7. Simulation results of the proposed DTT-5L-CMI with two cascaded modules (n = 2).

Fig. 8. Simulated THD and peak of output voltage (n = 1).

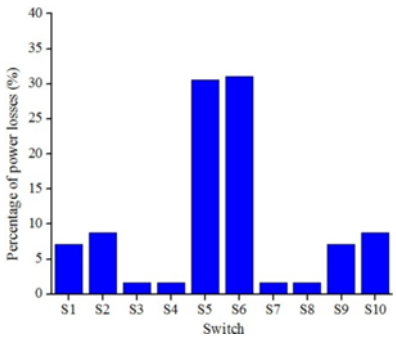


Fig. 9. Simulated power losses distribution for $M = 1$ ($n = 1$).

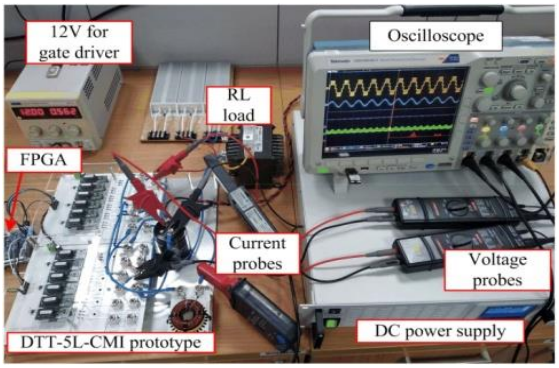
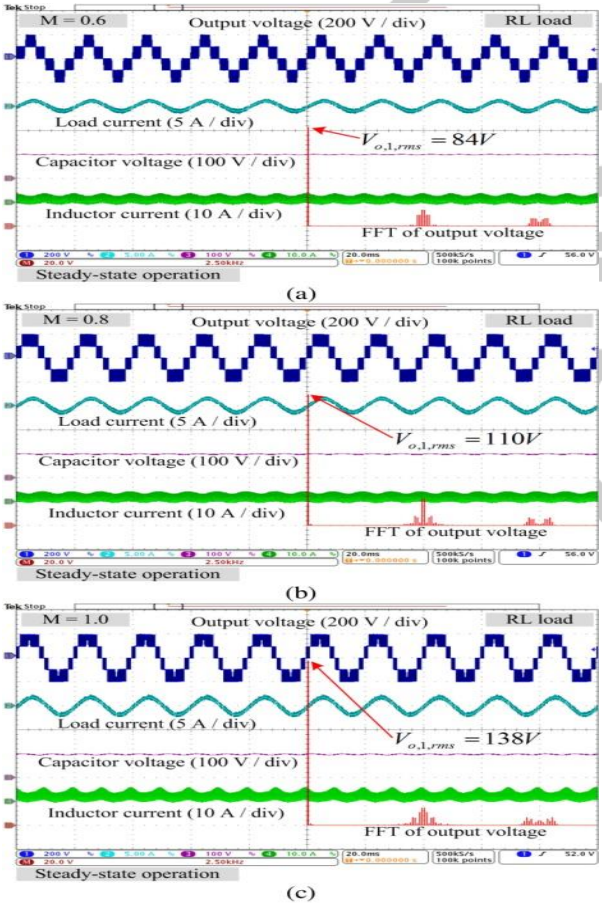


Fig. 10. Experimental setup of the proposed DTT-5L-CMI.

TABLE II
PROTOTYPE SPECIFICATION

Description	Value/Parameter
Input voltage, V_{dc}	100 V
Carrier frequency	5 kHz
Capacitor, C	1000 µF
Inductor, L	3 mH
Load resistor	100 Ω
Load inductor	0.1 H

Fig. 11. Steady-state waveforms of the proposed DTT-5L-CMI with *RL* load. (a) $M = 0.6$. (b) $M = 0.8$. (c) $M = 1.0$



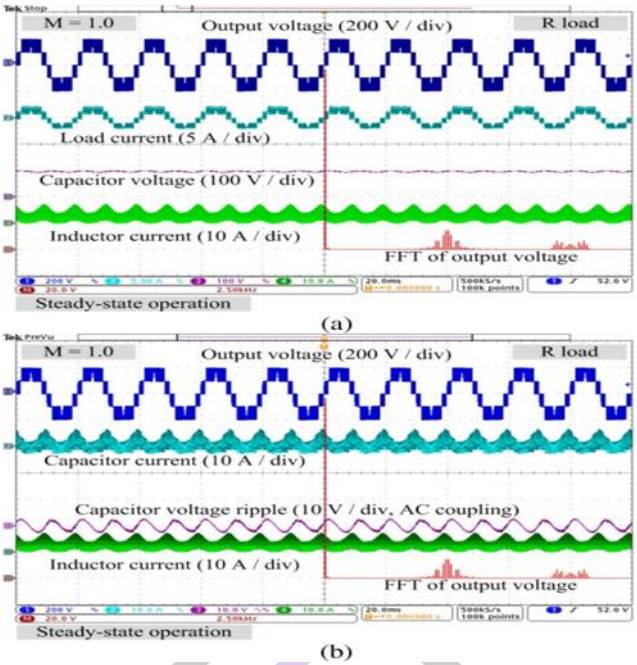


Fig. 12. Steady-state waveforms of the proposed DTT-5L-CMI with purely resistive load and $M = 1.0$.

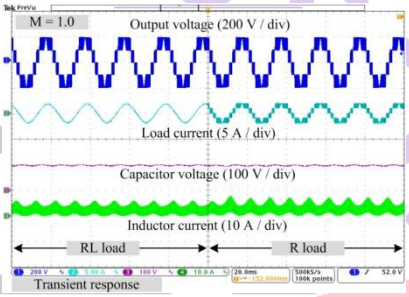
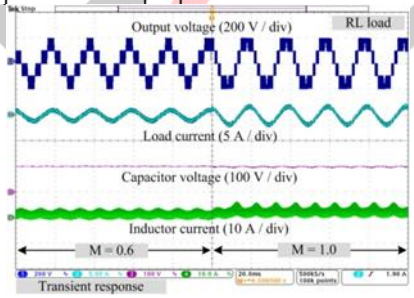


Fig. 13. Transient response of the proposed DTT-5L-CMI from *RL* load to *R* load

Fig. 14. Transient response of the proposed DTT-5L-CMI from $M = 0.6$ to $M = 1.0$.



Simulation was continued to study the performance of the proposed topology when practical power switches are taken into consideration. Power MOSFETs used in the experimental prototype were modeled accurately in PSIM software. Thermalmodule is used to perform curve fitting for the characteristic graphs specified in the datasheet. Using the same parameters asthose in the experimental prototype, the simulated output voltage that is supplying purely resistive load for different modulation indexes are analyzed and illustrated in Fig. 8. With single module($n = 1$), it is clear that the maximum voltage level is twice of theinput dc source, that is 200 V. It is also validated that the peakof output voltage for different M shows good agreement with (19), with the simulated values slightly less than the calculatedvalues. Besides, the total harmonic distortion (THD) of the output voltage is noted to be decreasing with M, while the maximum THD at $M = 0.2$ is as low as 1.5%.

A power losses analysis was then conducted at $M = 1$ where the simulated efficiency is approximately 99%. Fig. 9 shows the power losses distribution among the ten switches. Note that thepower losses of two switches in each half bridge (S1–S2, S5– S6, and S9–S10) are almost balanced. Therefore, the proposedtopology can also be implemented by using three half bridge modules with four additional switches.

EXPERIMENTAL RESULTS

For further validation, an experimental prototype was im- plemented and tested. Fast Fourier transform function of the oscilloscope

was used to compute the fundamental componentof the output voltage. The experimental setup and its corre- sponding specifications can be found in Fig. 10 and Table II, respectively. Fig. 11 shows the measured steady-state waveforms under inductive load. The load current is sinusoidal and the average capacitor voltage is 100 V for all modulation indexes.

Five voltage levels are generated between 200 and 200 V. It is clear that the magnitude of the fundamental output voltage is proportional to the modulation index with the measured value slightly less than the theoretical calculation using (19).

Experimental tests are then continued with purely resistive load, as shown in Fig. 12(a). The load current is proportional tothe voltage with five distinctive levels are observed. Fig. 12(b)demonstrates the corresponding plots when the oscilloscope channel was set to ac coupling. The measured capacitor voltageand current shows very good agreement with those obtained insimulation, thus further providing a proof of the operation andviability of the proposed topology.

Transient response of the experimental prototype was also conducted. In Fig. 13, smooth transition in load current is ob- served when the load is switched from *RL* to purely resistive load.The step change in modulation index from 0.6 to 1.0 in Fig. 14clearly shows that the magnitude of the load current increases instantaneously without affecting the average capacitor voltage.

CONCLUSION

In this article, a novel CMI topology is presented. Theoret- ical analyses were conducted and validated by simulation and experimental study of a prototype. The proposed DTT-5L-CMIis capable of five levels generation with double voltage boosting gain. Soft charging of capacitor and uniform operation for all cascaded modules are achieved that resolved the problems of recent SC-CMI. Therefore, the proposed topology is an attractive alternative for dc–ac power conversion system.

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