Multilevel Inverter Based Solar Application Using ANFIS MPPT

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***Abstract*: This paper proposes an Asymmetrical 21-level multilevel inverter topology for SEPIC converter provided to regulate the constant output voltage under various operating conditions based on solar application. Using the ANFIS MPPT algorithm, keep the converter's DC connection voltage constant. The PV voltage is boosted over the DC link voltage using a SEPIC converter interfaced in between the solar panels and the inverter. A 21-level inverter is employed and it converts the output of the SEPIC converter into AC supply and is tested experimentally with various combinational loads. Using the Multilevel inverter the THD is reduced and the quality of the output attained is also enhanced. The performance analysis of this technique is implemented in MATLAB/Simulink environment**.

Index Terms: **ANFIS MPPT algorithm, multilevel inverter, DC link, PV voltage**

I. INTRODUCTION

The demand for renewable energy has increased significantly over the years because of the shortage of fossil fuels and the greenhouse effect. Among various types of renewable energy sources, solar energy and wind energy have become very popular and demanding due to advancements in power electronics techniques. PV sources are used in many applications nowadays since they are low-maintenance and pollution-free. The voltage attained from the PV system is low, therefore for boosting the voltage, a DC-DC converter is employed

To improvise the quality of the desired output, the output from the DC-DC converter is fed to a multilevel inverter. The MLI converts the dc power obtained into ac power and is fed into the load. The enhancement in the output waveform of the inverter reduces its harmonic content, the size of the filter used, and the levels of electromagnetic interference (EMI) generated by the switching operation of the inverter. Multilevel inverters have gained popularity in recent years due to their advantages over traditional three-level inverters. The MLI offers improved output waveforms, smaller filter size, lower EMI, and, lower total harmonic distortion (THD).

Because of lower total harmonic distortion (THD), lower switching stress, and lower electromagnetic interference, multilevel inverters are recommended solutions for photovoltaic (PV) applications (EMI). A five-level transformer-less inverter is proposed to reduce the leakage current in the single-phase low-power PV inverters [1]. A new constraint is established for the two switching angles to derive the formula for the harmonics' amplitude, resulting in the self-elimination of all triple harmonics. The fifth and seventh harmonic orders are mitigated through the normal operation of the proposed SHM-PAM technique [2]. To increase the DC bus voltage utilization of the inverter nearly to that of the six-step mode of operation using a single CHB unit per phase [3]. The inverter is a programmed single-phase current source inverter. Only five switches are required to obtain the configurable level output It has the advantages of a simple structure and programmable level output, as opposed to the conventional single-phase reduced-count multilevel inverters [4]. A five-level common ground Transformer-less inverter with reduced output harmonic content for PV systems is proposed. In addition, the proposed inverter can process reactive power and it presents a maximum dc-voltage utilization in opposition to half-bridge-based topologies [5]. A multi-cell configuration of DC-switched capacitor cells generates the variable DC-link, and numerous DC-cells at the DC-link can increase the number of voltage levels created on the AC side. without proportionally increasing the number of active and passive devices [6]. An optimal controller, based on a linear quadratic regulator with integral action, is designed to inject a sinusoidal current with low harmonic distortion at a unity power factor [7]. Transformer-less five-level inverter with zero leakage current and the ability to reduce the harmonic output content for a grid-tied single-phase PV system. The grid's neutral connects to a common, to which the DC-negative links and positive terminals are connected through parasitic capacitors to avoid leakage current [8]. Five-level transformer-less inverter topology is proposed to eliminate the leakage current based on the principle of the switched capacitor. Besides, the proposed topology has naturally balanced voltage capability, so no dedicated control strategy/algorithm is required for balancing/regulating the flying capacitor voltages [9]. The net dc-bus voltage will be spread evenly between four dc-bus capacitors in the series-connected multilevel inverter. Therefore, the converter generates a multilevel voltage waveform with uniform steps and ensures equal voltage stress on the semiconductor devices [10]. Hector to improvise the quality of the desired output, the output from the DC-the converter is fed to a multilevel inverter. The MLI converts the dc power obtained into ac power and is fed into the load. The enhancement in the output waveform the of inverter reduces its harmonic content, size of the filter used, and the level of electromagnetic interference (EMI the) generated by the switching operation of the inverter. To enhance the maximum power from the PV system, the ANFIS MPPT algorithm is used for both the output and the voltage of the PV system. SEPIC Converter is used to generate desired output voltage levels with a low THD.

II. PROPOSED SYSTEM

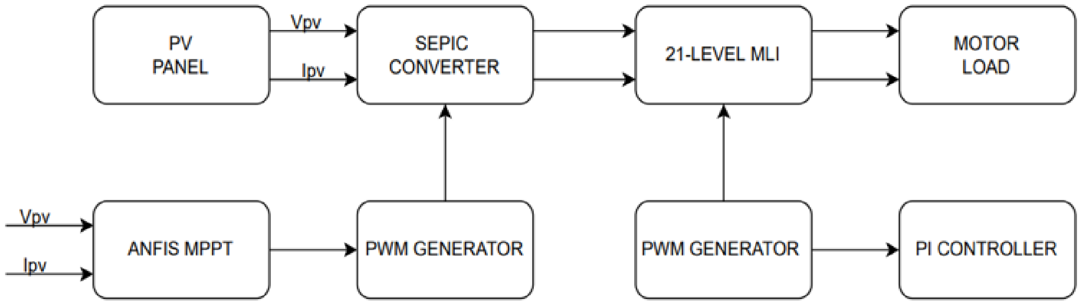


Figure 1 proposed block diagram

The demand for renewable energy has increased significantly over the years because of the shortage of fossil fuels and the greenhouse effect. Among various types of renewable energy sources, solar energy and wind energy have become very popular and demanding due to advancements in power electronics technique interference (EMI)asymmetrical 21-level multilevel inverter topology is used in the SEPIC converter based solar application Photo Voltaic (PV) sources are used today in many applications as they have the advantages of being maintenance and pollution free. The voltage attained from the PV system is low, therefore for boosting the voltage, a DC-DC converter is employed. To improvise the quality of the desired output, the output of the DC converter is fed to a multilevel inverter. The MLI converts the dc power obtained into ac power and is fed into the load. The enhancement in the output waveform of the inverter reduces its harmonic content, the size of the filter used, and the level of electromagnetic interference (EMI) the generated by switching operation of the inverter.

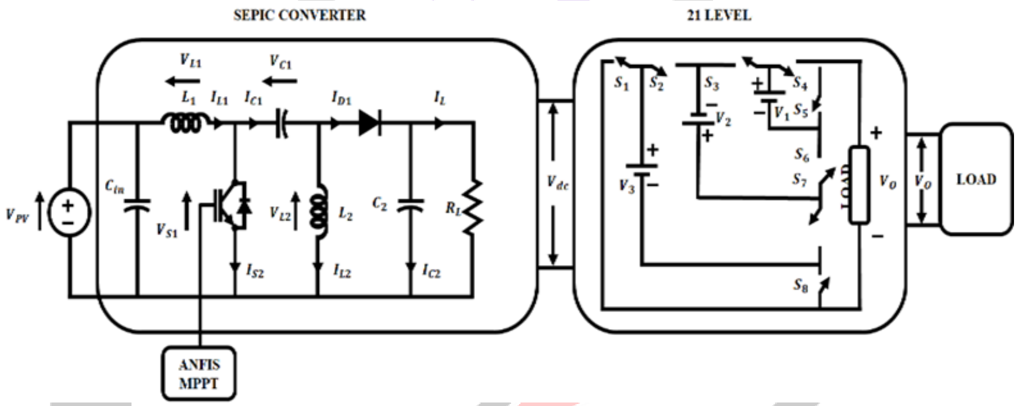


Figure 2 proposed circuit diagram

A novel asymmetrical 21-level multilevel inverter topology is used in the SEPIC converter-based solar application. The low voltage DC output of PV is boosted with the aid of a SEPIC converter. The 21-level multilevel inverter converts the DC output of the converter into AC voltage. The output of the Inverter is then fed to the ANFIS-powered MPPT technique is implemented to extract the maximum power from the solar panels. Regardless of partially shadowed situations, stable production is produced. In the proposed 21-level symmetrical MLI, the switches are selected based on the strategy of avoiding short circuits in the specified path of current traversal.

A) PV SYSTEM

The PV module and load conditions. Hence to increase the derivation of power from the PV module, optimal power point operation of the module is important. This controller, known as the maximum power point tracker, is required. PV cells are manufactured from different materials. The PV system used for power conversion consists of several series and parallel combinations of the PV modules the tracking controller and power converters like DC-DC converter The sun is a renewable energy source that is both environmentally beneficial and long-lasting The energy radiated from the sun is received directly for power generation by way of photovoltaic. One of the significant methodologies utilized from solar power is photovoltaic (PV) which is capable of converting sunlight into electricity using the photovoltaic effect. The basic building block of photovoltaic modules which produces electricity from the light energy by photovoltaic effect is a Solar cell. The efficiency of a PV module is determined by the material used in photovoltaic cells and the method used to assemble the solar cells into a module. The efficiency of the module is about 12-29 % in the conversion of sunlight to electric energy. Among this gallium Arsenide, solar cells have 29% of maximum efficiency, whereas solar cells have 12-14% of efficiency. The performance of the PV module may also drop due to Temperature in and inverter. Hence the generated DC voltage can be amplified using a DC-DC converter and converted to AC by using the inverter. The PV panel should be chosen based on the load rating.

The PV cell's electrical original diode model is as follows

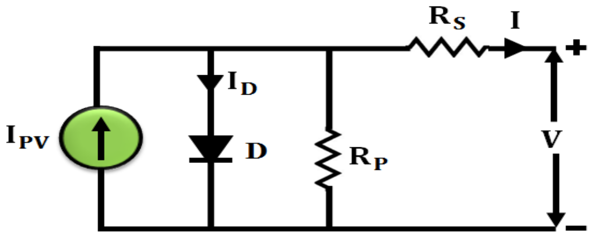


Figure 3 Equivalent circuit of PV cell

The PV model constitutes current sources, diode Shunt resistance Rsh, Series Resistance Rs. Shunt Resistance represents present the cell face leakage through the edges.

The total current I is the difference between the light-generated current Iph, diode current Id, and current through Rph.

$I = I_{ph} - I_d - I_{sh}$ (1)

Equations (2) and (3) show the diode current Id and the shunt resistance current Ish (3)

$I_d = I_0\left\{\exp\left[\frac{q}{mkT_c}(V + IR_s)\right] - 1\right\}$ (2)

$I_{sh} = \frac{V+IR_s}{R_{sh}}$ (3)

m = Idealizing factor

K = Boltzmann constant

T c = Absolute temperature of cell

q = Charge of electron

V = Implicit across cell

I_0= Cell reverse saturation current

By exercising Equations is shown in below

$I = I_G - I_0\left\{exp\left[\frac{q}{mkT_c}(V + IR_s)\right]1\right\}\frac{V+IR_s}{R_{sh}}$ (4)

Generally, Shunt Resistance R_sh in PV cells is high. Hence(VIR_s)/R_sh is excluded Hence,

$I = I_G - I_0\left\{exp\left[\frac{V+IR_s}{A}\right] - 1\right\}$ (5)

Where A = wind befitting parameter

A = (mkT_c)/ q (6)

Determination of phase current I_ph According to Figure 4.1 affair current at standard test condition is

$I = I_{ph} - I_0\left[exp\left(\frac{V}{a}\right) - 1\right]$ (7)

When PV cell is short circumvented

$I_{sc} = I_{ph} - I_0\left[exp\left(\frac{0}{a}\right) - 1\right]$ (8)

Only in the ideal case Equation (4.8) is valid. Hence the equivalency isn't accurate. Equation (4.9) is written as

$I_{ph} \approx I_{sc}$ (9)

Both irradiance and temperature affect the photocurrent.

$I_{ph} = \frac{G}{G_{ref}}(I_{ph} + \mu_{sc}.\Delta T)$ (10)

G = irradiance at standard testing conditions

Determination of I_0

The shunt resistance is generally high for all operations and hence excluded by using 3 standard conditions

Open circuit voltage (I = 0, V = V_oc)

Short circuit current(V = 0, I = I_sc)

The voltage(V_mp) and current(I_mp) at maximum power in the following equation are written as

$I_{sc} = I_{ph} - I_0\left[exp\left(\frac{I_{sc}.R_s}{A}\right) - 1\right]$ (11)

$O = I_{ph} - I_0\left[exp\left(\frac{V_{oc}}{A}\right) - 1\right]$ (12)

$I_{pm} = I_{ph} - I_0\left[exp\left(\frac{V_{pm}+I_{pm}R_s}{A}\right) - 1\right]$ (13)

Term (- 1) is excluded as it's veritably small compared to exponential term. According to Equation (10) substituting (I_ph) in Equation(13)

$0 \approx I_{sc} - I_0 exp\left(\frac{V_0}{A}\right)$ (14)

$I_0 = I_{sc}\ exp\left(\frac{-V_{0c}}{A}\right)$ (15)

B) SEPIC CONVERTER

By regulating the Duty Cycle of a pulse to the MOSFET, the SEPIC converter can increase or decrease an input voltage. One way to do that is to directly control the Duty cycle using a potentiometer SEPIC is a DC-DC converter allowing the yield voltage to be not exactly, more than, from for its information. The yield of the SEPIC is worked through the commitment Pattern of the oversee transistor. SEPIC is ordinarily a lift converter and it is seen by utilizing a buck-raise converter. Thus it's far from a normally finished method for a greenback-raise converter, it has the advantage of having a non-modified yield (the yield that has indistinguishable voltage polar as the enter). To move a chain capacitor to couple power from the contribution to the yield (and to react in a more style to a concise circuit yield), and to have the capacity to do chevalier of concerned shutdown: after the switch S1 is developed to get off, its yield drops to 0 V, following an ephemeral withdraw of charge.

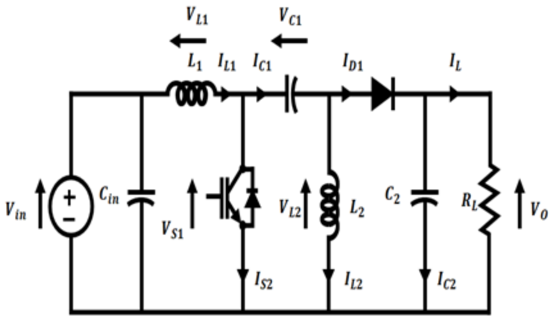


Figure 4 SEPIC Converter Block Diagram

SEPIC is advantageous in applications in which a battery voltage can be above and underneath that of the controller's design yield. The schematic diagram for a basic SEPIC appears in the parent because they did exchange mode power components (uncommonly DC-to-DC converters). The SEPIC impact power among the capacitors and inductors is to substitute starting with one voltage and then onto the next. The traded measure of vitality is approved in switch S1, which is a transistor that includes a MOSFET. A SEPIC converter is also called a single-ended primary inductor converter. It is based on a dc-dc converter with several inputs. The polarity of the output voltage cannot be changed for a step up and step down the capability of a converter and a series capacitor is used to couple energy from the input to its output. A SEPIC is essentially a boost converter followed by an inverted buck-boost converter, thus it's identical to a typical buck-boost converter. However, the benefits of having a SEPIC outweigh the disadvantages. Non-inverted series capacitor couples energy from the input to the output (the output has the same voltage polarity as the input).MOSFET is more noteworthy higher a decent arrangement rivalry to the current day and lower voltage drop than bipolar intersection transistors (BJT). It does now not requires biasing resistors as MOSFET exchanging is overseen through contrasts in voltage instead of the present day.

C) ANFIS based MPPT

A new ANFIS-based MPPT method is proposed to achieve tracking the maximum power of the PV module underchanging weather conditions. The proposed input variables are the PV voltage (V_ PV), PV current (I_ PV), and the PV cell temperature (TPV). The output variable is the duty cycle, which is used to control the DC-DC switched SEPIC converter to keep tracking maximum power. Because traditional FLC modeling is dependent on trial and error, the chances of achieving ideal performance are slim.

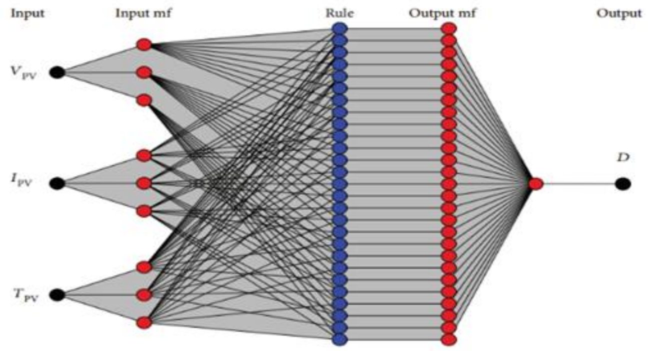


Figure 5 ANFIS model structure.

As a result, learning ANFIS can be used to obtain membership functions and fuzzy rules. The trained data should be collected first. To obtain the trained data, the steps involved are as follows,

Using traditional MPPT methods, the system was simulated under various sun radiation and temperature conditions

The data was collected and processed using a MATLAB algorithm that was created specifically for this purpose.

The manipulated data were then shuffled. The data is then filtered again to extract only the unique rows in the data collection.

D) 21-LEVEL INVERTER

Multilevel Inverters [MLI] are devices that use power electronic switches, power diodes, and some DC voltage to generate a stepwise output waveform. The source could be PV cells connected in series or parallel, a renewable energy source, or a battery. Multilevel inverters reduce DV/it strains on equipment while also producing low harmonic distortion. Electromagnetic compatibility can be reduced as a result. In MLIs, there are three basic types of topologies. Diode clamped, Flying Capacitor, and Cascaded Multilevel Inverters are the three types. In diode clamped MLI, a diode transfers a limited amount of voltage, reducing the load on other electrical devices. Half of the input DC voltage is used as the maximum output voltage. The neutral point clamped (NPC) inverter was another name for the inverter. The structure of the multilayer inverter is based on the series connection of each Sub cell. The flying capacitor was initially introduced by Meynard. The inner redundancies in this topology are redundant. Two or more legitimate switch combinations can produce the voltage levels; in other terms, two or more valid switch combinations can produce the voltage levels. The waveform of the required output voltage MLIs with cascaded H Bridges can be symmetrical or asymmetrical.

The kind that is asymmetrical All of the voltage sources utilized in a symmetrical cascaded H-Bridge are of the same type. In symmetrical, the voltage sources employed are of the same magnitude, but in asymmetrical, the voltage sources are of unequal magnitude. The multilevel converter is made up of nine switches (IGBT) that are activated by three sources located nearby. MLI's synthesized output can be obtained using with the help of the switching, providing multiple channels for conduction to the connected sources. The power switch pattern. For the sources, a variation in values might be considered. Therefore, The proposed solution is broken down into two sections: symmetrical and asymmetrical structure. Another key element of the aforementioned structure is its modularity, which allows it to be customized. The output changes with the same architecture when utilized in high-voltage applications. The 21-level MLI converts the input DC signal into an AC signal in the defined work, resulting in a higher-quality output waveform with lower THD, which is then sent to the motor load.

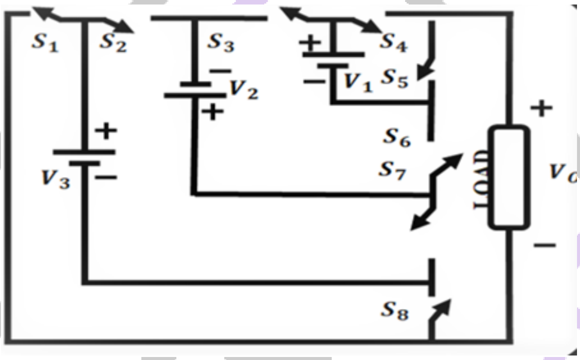


Figure 7 Multilevel inverter

III. RESULT

The simulation results are examined using the software MATLAB/SIMULINK.

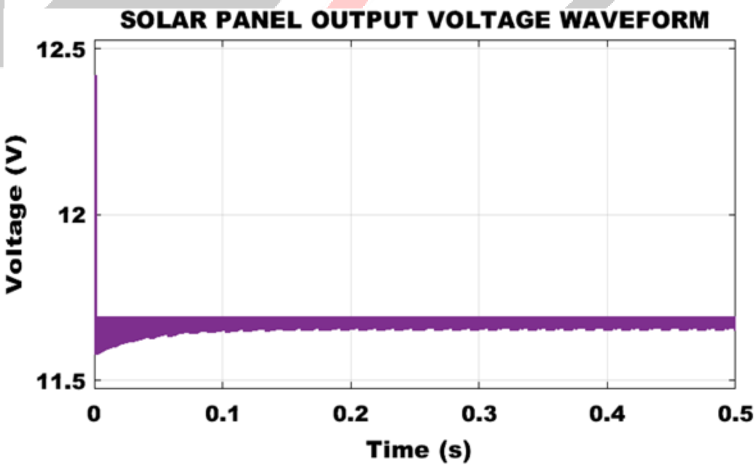


Figure 7 Solar panel output voltage waveform

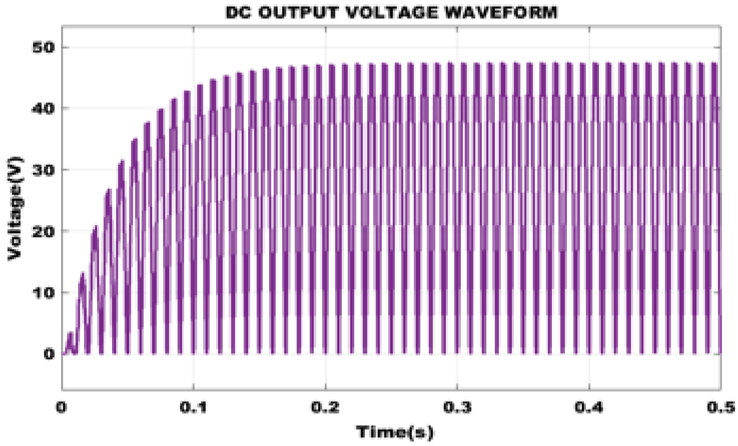


Figure 8 Output Voltage Waveform

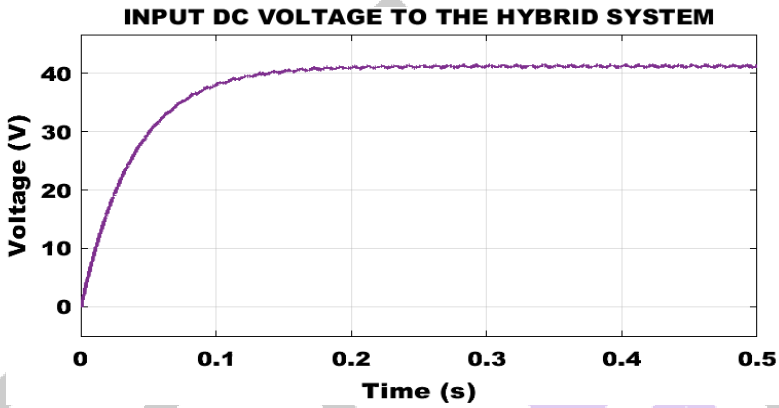
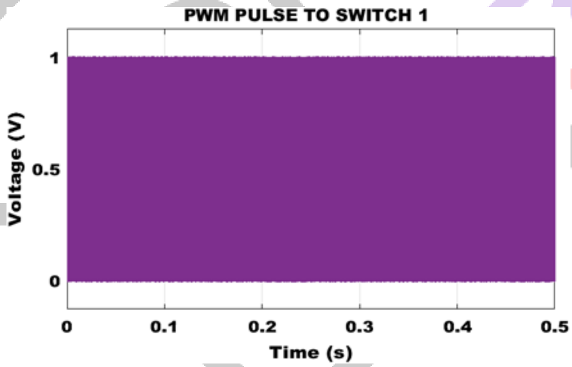
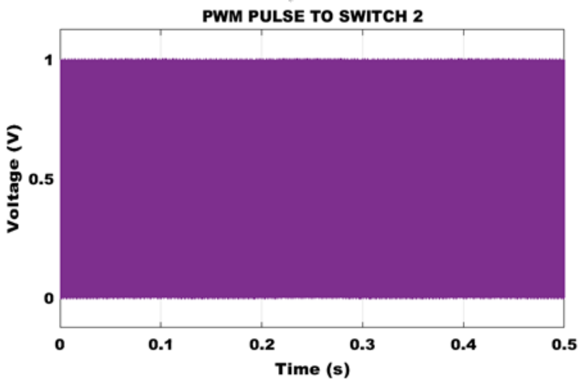


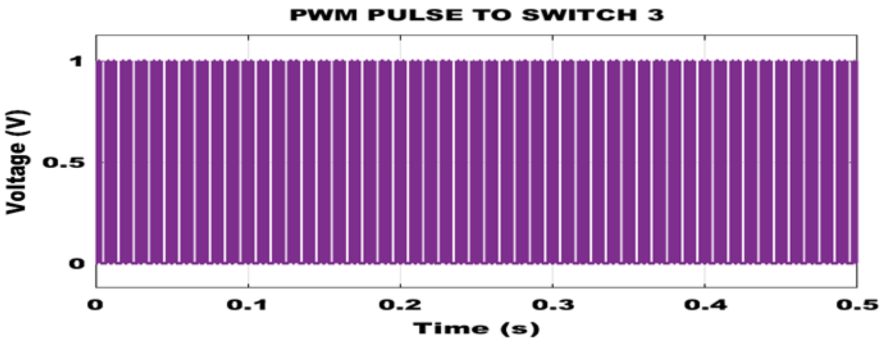
Figure 9 Input DC Voltage to the Hybrid System



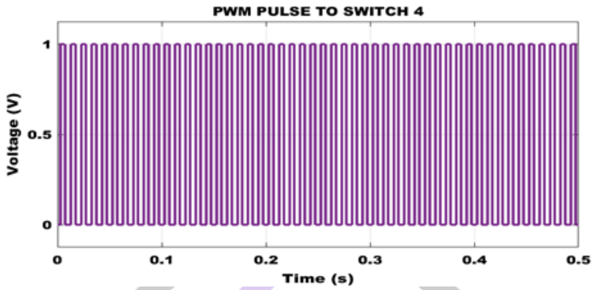
10(a)



10(b)

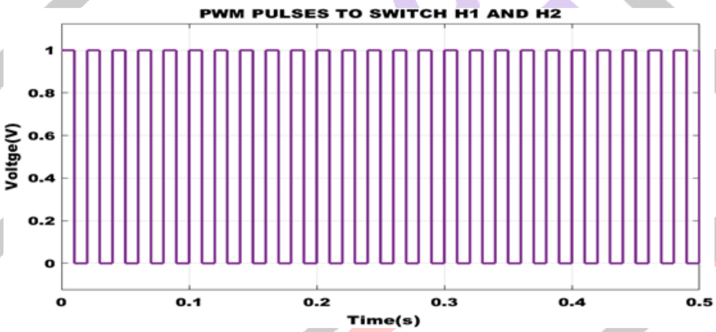


10(C)

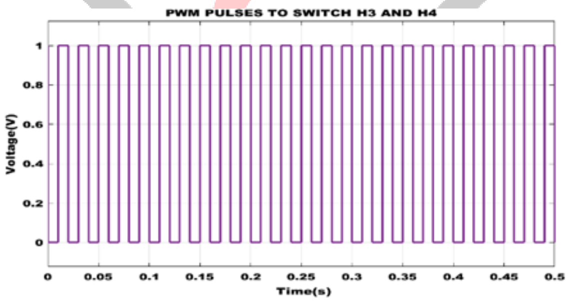


10 (d)

Figure 10 PWM pulse to switch waveform Figures 10 (a, b, c, d) indicates the PWM pulse applied to switches S1, S2, S3, and S4 respectively. A constant pulse of 1V is applied to the switches for the effective control of the operation



11(a)



11(b)

Figure 11 (a) & (b) PWM Pulse to Switch H1 and H2

Figures 11 (a) & (b) indicate the PWM pulse applied to the terminals H1, H2, H3, and H4. A constant pulse of 1V is applied for controlling the operation of the converter.

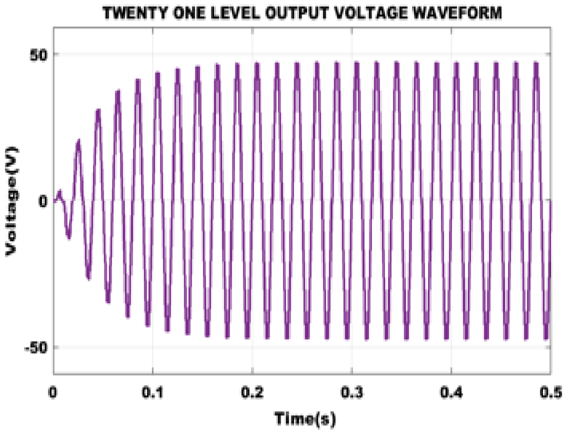


Figure 12 Twenty one level output voltage waveform

The voltage value ranges from +50V to -50V for a varying period of seconds.

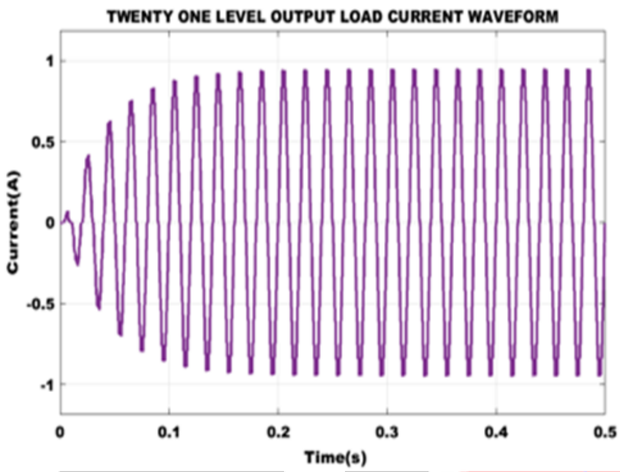


Figure 13 Twenty One Level Output Load Current Waveform

The output current waveform for the 21-level inverter is shown in Figure 13. The current value ranges from +1A to -1A for a varying period of seconds.

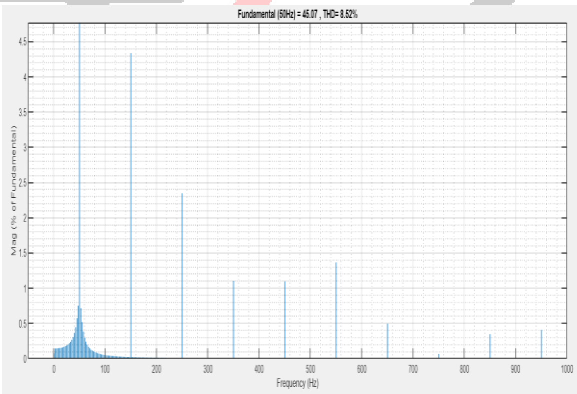


Figure 14 21 level inverter THD waveform

Figures 14 represent the THD waveforms of the 21-level inverter. The obtained values for the THD are given by 8.52%. Thus the proposed approach generates improved voltage outputs with minimized THD.

Figure 15 Hardware view

IV. CONCLUSION

A new 21-level inverter has been designed with a reduced number of components for solar PV applications was proposed in this project. The conventional SEPIC converter produces a higher DC-link voltage and is fed to the inverter for AC stepped output waveform. ANFIS-based MPPT technique is implemented to extract the maximum power from the PV panel, the stable output is achieved irrespective of partially shaded conditions. The 21-level multilevel inverter generates higher output voltage levels with a lesser number of circuit components with low THD. The DC voltage source was provided with reduced losses, high efficiency, and total harmonic distortion is found to be relatively low

REFERENCES

1. Xiaonan Zhu; Hongliang Wang; Wenyuan Zhang; Hanzhe Wang; Xiaojun Deng; Xiumei Yue,2020, "A novel single-phase five-level transformer-less photovoltaic (PV) inverter", CES Transactions on Electrical Machines and Systems, vol: 4, no: 4, pp. 329 – 338.
2. Mohammad Sharifzadeh; Hani Vahedi; Ramon Portillo; Leopoldo Garcia Franquelo; Kamal Al-Haddad,2019, "Selective Harmonic Mitigation Based Self-Elimination of Triple Harmonics for Single-Phase Five-Level Inverters", IEEE Transactions on Power Electronics, vol: 34, no: 1, pp. 86 – 96.
3. Teemu Techela Davis; Anubrata Dey, 2019, "Investigation on Extending the DC Bus Utilization of a Single-Source Five-Level Inverter With Single Capacitor-Fed H-Bridge Per Phase", IEEE Transactions on Power Electronics, vol: 34, no: 3, pp. 2914 – 2922.
4. Xiaoqiang Guo; Yu Bai; Baocheng Wang,2019, "A Programmable Single-Phase Multilevel Current Source Inverter", IEEE Access, vol: 7, pp. 102417 – 102426.
5. Felipe Bovolini Grigoletto, 2020, "Five-Level Transformer-less Inverter for Single-Phase Solar Photovoltaic Applications", IEEE Journal of Emerging and Selected Topics in Power Electronics, vol: 8, no: 4, pp. 3411 – 3422.
6. Md Noman Habib Khan; Mojtaba Forouzesh; Yam P. Siwakoti; Li Li; Frede Blaabjerg,2020, "Switched Capacitor Integrated (2n + 1)-Level Step-Up Single-Phase Inverter",IEEE Transactions on Power Electronics, vol: 35, no: 8,pp. 8248 - 8260.
7. Naima Arab; Hani Vahedi; Kamal Al-Haddad,2020, "LQR Control of Single-Phase Grid-Tied PUC5 Inverter With LCL Filter", IEEE Transactions on Industrial Electronics, vol: 67, no: 1, pp. 297 – 307.
8. Ahmad H. Sabry; Zeina Mueen Mohammed; Farah Hani Nordin; N. H. Nek Ali; Ali Saadon Al-Ogaili,2020, "Single-Phase Grid-Tied Transformer-less Inverter of Zero Leakage Current for PV System", IEEE Access, vol: 8, pp. 4361 – 4371.
9. Naser Vosoughi; Seyed Hossein Hosseini; Mehran Sabahi, 2020, "A New Transformer-Less Five-Level Grid-Tied Inverter for Photovoltaic Applications", IEEE Transactions on Energy Conversion, vol: 35, no: 1, pp. 106 – 118.
10. Apparao Dekka; Omid Beik; Mehdi Narimani, 2020, "Modulation and Voltage Balancing of a Five-Level Series-Connected Multilevel Inverter with Reduced Isolated Direct Current Sources", IEEE Transactions on Industrial Electronics, vol: 67, no: 10, pp. 8219 – 8230.
11. R. S. Alishah, S. H. Hosseini, E. Babaei, and M. Sabahi, ''A new general multilevel converter topology based on the cascaded connection of Sub multilevel units with reduced switching components, DC sources, and blocked voltage by switches,'' IEEE Trans. Ind. Electron., vol. 63, no. 11, pp. 7157–7164, Nov. 2016
12. K. K. Gupta and S. Jain, ''A novel multilevel inverter based on switched DC sources,'' IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3269–3278, Jul. 2014.
13..P. Omer, J. Kumar, and B. S. Surjan, ''A review on reduced switch count multilevel inverter topologies,'' IEEE Access, vol. 8, pp. 22281–22302, 2020. [17] C. Verdugo,
14.T. Noguchi, S. Togashi, and R. Nakamoto, ''Short-current pulse-based maximum-power-point tracking method for multiple photovoltaic converter module systems,'' IEEE Trans. Ind. Electron., vol. 49, no. 1, pp. 217–223, Aug. 2002.
15..C. Verdugo, J. I. Candela, and P. Rodriguez, ''Energy balancing with a wide range of operation in the isolated multi-modular converter,'' IEEE Access, vol. 8, pp. 84479–84489, 2020.
16.. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, ''Multilevel inverter topologies with reduced device count: A review,'' IEEE Trans. Power Electron., vol. 31, no. 1, pp. 135–151, Jan. 2016.

17. Y. Suresh and A. K. Panda, ''Investigation on hybrid cascaded multilevel inverter with reduced DC sources,'' Renew. Sustain. Energy Rev., vol. 26, pp. 49–59, Oct. 2013.
18. C. Balakishan, N. Sandeep, and M. V. Aware, ''Design and implementation of three-level DC-DC converter with golden section search based MPPT for the photovoltaic applications,'' Adv. Power Electron., vol. 2015, pp. 1–9, Feb. 2015.
19. A. Stonier, S. Murugesan, R. Samikannu, S. K. Venkatachary, S. S. Kumar, and P. Arumugam, ''Power quality improvement in solar fed cascaded multilevel inverter with output voltage regulation techniques,'' IEEE Access, vol. 8, pp. 178360–178371, 2020.
20. N. Bizon, ''Global extremum seeking control of the power generated by a photovoltaic array under partially shaded conditions,'' Energy Convers. Manage., vol. 109, pp. 71–85, Feb. 2016.
21. E. Babaei, S. Laali, and Z. Bayat, ''A single-phase cascaded multilevel inverter based on a new basic unit with a reduced number of power switches,'' IEEE Trans. Ind. Electron., vol. 62, no. 2, pp. 922–929, Feb. 2015.
22. S. N. Singh, ''Selection of non-isolated DC-DC converters for solar photovoltaic system,'' Renew. Sustain. Energy Rev., vol. 76, pp. 1230–1247, Sep. 2017. [12] A. B. G. Bahgat
23.Y. Yang and H. Wen, ''Adaptive perturb and observe maximum power point tracking with current predictive and decoupled power control for grid-connected photovoltaic inverters,'' J. Mod. Power Syst. Clean Energy, vol. 7, no. 2, pp. 422–432, Mar. 20192
24. P. Ponnusamy, P. Sivaraman, D. J. Almakhles, S. Padmanaban, Z. Leonowicz, M. Alagu, and J. S. M. Ali, ''A new multilevel inverter topology with reduced power components for domestic solar PV applications,'' IEEE Access, vol. 8, pp. 187483–187497, 2020.
25. M. N. Bhukya, V. R. Kota, and S. R. Depuru, ''A simple, efficient, and novel standalone photovoltaic inverter configuration with reduced harmonic distortion,'' IEEE Access, vol. 7, pp. 43831–43845, 2019.
26. N. Asim, K. Sopian, S. Ahmadi, K. Saeedfar, M. A. Alghoul, O. Saadatian, and S. H. Zaidi, ''A review on the role of materials science in solar cells,'' Renew. Sustain. Energy Rev., vol. 16, no. 8, pp. 5834–5847, 2012.
27. M. G. Villalva, J. R. Gazoli, and E. R. Filho, ''Comprehensive approach to modeling and simulation of photovoltaic arrays,'' IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1198–1208, May 2009.
28. K. Leban and E. Ritchie, ''Selecting the accurate solar panel simulation model,'' in Proc. Nordic Workshop Power Ind. Electron. (NORPIE). Espoo, Finland: Helsinki Univ. Technology, Jun. 2008, pp. 1–7.