IMPLEMENTATION of DIGITAL CLOCK WITH STOPWATCH on FPGA

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***Abstract*- The industry standard for real-time operations and linear control systems today is FPGA (Field Programmable Gate Array)-based implementation. The objective here is to build a digital clock with stopwatch using Verilog and either the FPGA i.e., Zed board. The system that will be constructed will have a 6-digit clock with hour, minute, and second hands utilizing extremely affordable equipment that will be placed in an ideal location. The design has every component that a digital clock should have, and because it is synchronous, the overall latency is minimal. The Software "Xilinx Vivado" is used to implement a Verilog HDL code that is used to design the notion mentioned above.**

***Index Words*- Control systems, FPGA, Verilog, Zed board, Synchronous, Latency, Xilinx Vivado**

I. INTRODUCTION:

A digital clock with a stop watch on FPGA is an electronic device that displays the current time in a digital format using a set of LEDs or seven-segment displays [1]. Additionally, it can also have a stopwatch functionality that allows users to measure elapsed time. Such devices are often designed using FPGAs (Field Programmable Gate Arrays) due to their versatility and ability to be programmed and reprogrammed as needed.

The FPGA usually comprises a crystal oscillator to provide a stable reference frequency for the clock, a counter to keep track of time, and a multiplexer to select and display the appropriate digits on the LED or seven-segment display. The stopwatch module comprises a set of buttons to control the start, stop, and reset functions, along with a counter to measure and display elapsed time.[1]

FPGAs offer many advantages over traditional clock and stopwatch circuits, like increased flexibility, speed, and reliability. The clock and stopwatch functionalities can be integrated into a single FPGA design, reducing component count, size, and complexity, making it an ideal choice for applications that require both clock and stopwatch functionalities. Additionally, the FPGA can also be used to implement additional features like alarm clocks or timer functions.

II. LITERATURE SURVEY:

A digital clock with stopwatch is a common application of Field Programmable Gate Array (FPGA). Here are some relevant literature reviews on this topic:

The survey describes the design and implementation of a stopwatch based on an FPGA. The FPGA is programmed with Verilog HDL and the stopwatch is implemented with a state machine. The design includes a 12-hour clock display, a stopwatch with lap function and an alarm clock. The design is tested on a Xilinx Spartan-6 FPGA.[2]

The proposed model introduces the design and implementation of a digital clock using an FPGA. The Verilog HDL is used to program the FPGA and the design includes a 12-hour clock display with AM/PM indication a stopwatch, and an alarm clock. The design is tested on a Xilinx Spartan-3E FPGA.[3]

The review suggests that the design and implementation of a digital clock with a stopwatch on an FPGA [4] is a popular topic. The designs typically include clock display, stopwatch function and alarm clock functions and are implemented with either VHDL or Verilog HDL. Designs are tested on various FPGA platforms such as Xilinx Spartan-3E, Spartan-6, etc.

III. DESIGN OVERVIEW & IMPLEMENTATION:

Design methodology:

A top-down approach is used in system design. This system primarily serves as a stopwatch and a digital clock. A counter is used to implement these functions i.e., digital clock module, stopwatch module, and a display module. Digital clock module uses an internal clock signal that updates the hours and minutes count. Upon each counter's completion, an internal clock signal is produced, and the subsequent counter updates it. Stop watch module will display up to 59 seconds and then return backs to 00 seconds. Three buttons, labelled start, stop, and pause, are provided for control. Display module is a common anode display which uses a Pmod (peripheral module interface) seven segment for display. There is a switch that allows you to switch between a stopwatch and a digital clock. All the modules are combined in the top module.

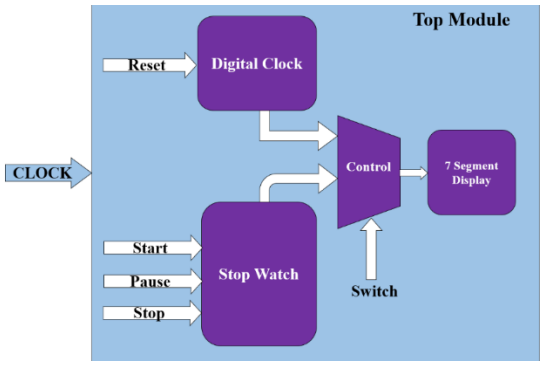

Fig.1 Block of Digital Clock with StopWatch

The block diagram is designed in such a way that, the output of the digital clock and stopwatch is multiplexed. By using a select line as switch, the selection of desired output among digital clock and a stop watch is displayed on seven segment display.

Software implementation:

Xilinx Vivado Design Suite is a software suite produced by Xilinx for the synthesis and analysis of hardware description language (HDL) designs used for the development of the complete system. Verilog, a hardware description language is used in writing the code for the implementation of the digital-clock and stopwatch.

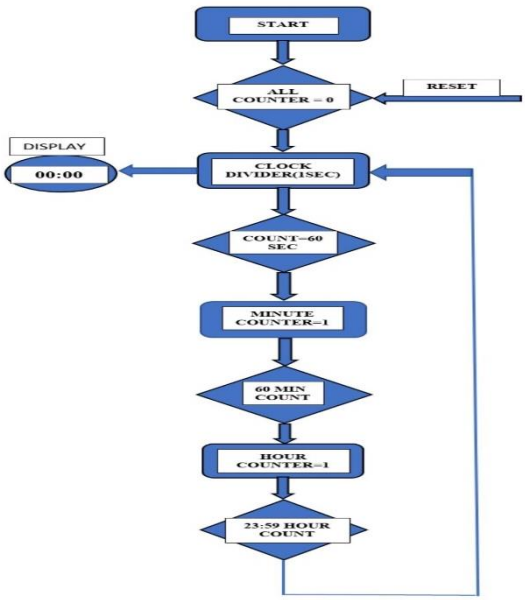

Fig. 2 Flowchart for Digital Clock

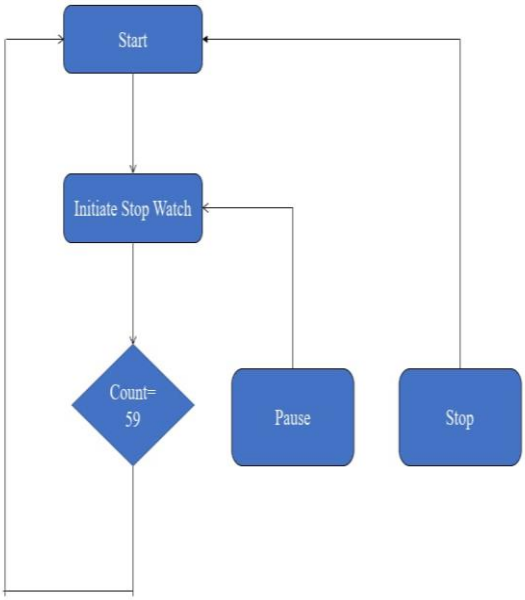

Fig.3 Flowchart for Stopwatch

Hardware Implementation:

- FAMILY: Zed Board Zynq-7000
- DEVICE: XC7Z020
- PACKAGE: CLG484
- SPEED: -1

PMOD SSD (Peripheral Module Interface Seven Segment Display): The seven pins used to control each display's seven segments are shared by the two-digit displays. To show both digits, we must switch between them more quickly than the eye can register.

The hardware implementation of a digital clock along with a stopwatch can be achieved here using FPGA. The clock operation starts as soon as the FPGA is switched on. Time signals are generated by the integrated clock and the FPGA. The time and stopwatch can be selected using the switches on the circuit board. Counting, incrementing, and decrementing are some of the digital operations used to improve the proposed digital clock design. Minutes and hours can be changed using the switches on the circuit board. The integrated 100 MHz crystal oscillator ensures a stable and high-frequency clock.[4] The frequency divider block thereby divides the frequency up to one hertz (Hz). This results in the base count for the entire design being the one-second count. The digital clock is reset to 00:00 and starts counting again when the counter reaches 23 hours and 59 minutes.[4]

The time is displayed on a digital clock. Instead of the rotating mechanism of electromechanical watches, digital counters are used to display seconds, minutes, and hours.[4] The 1 second pulse from the counter module is provided as an input to the stopwatch and digital clock modules.[5] When the start switch is turned on, the stopwatch starts counting immediately. In addition, the digital clock module starts counting seconds. Every minute consists of 60 seconds and every hour consists of 60 minutes. After twenty-four hours, the digital clock is reset to zero. Separate switches are provided for starting and stopping a stopwatch. The longest

possible count for the stopwatch is 60 seconds. The display module (PMOD Seven-Segment Displays) displays either a stopwatch or a digital clock, depending on the switch (Input control).

IV. RESULT:

The objectives we had set for ourselves for this were successful. The digital clock with stopwatch simulation performed by our code ran without errors and successfully mimicked the actual one. All the additional user interaction functions that we added performed as intended. We tested our code at each stage to ensure that everything was correctly mapped. By using different coding techniques and different parameters the output of the digital clock and stopwatch has been implemented on the Zed board. A switch as control is used to access both features. And start, stop, and pause are used to control the stopwatch individually.

Outputs:

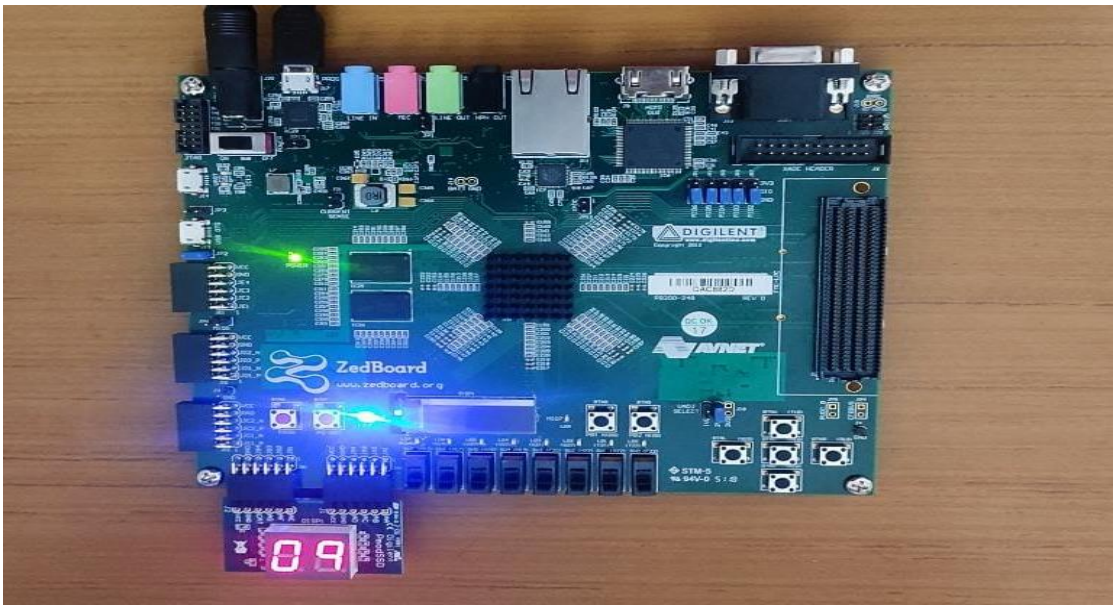

Fig. 4 Zed board Output

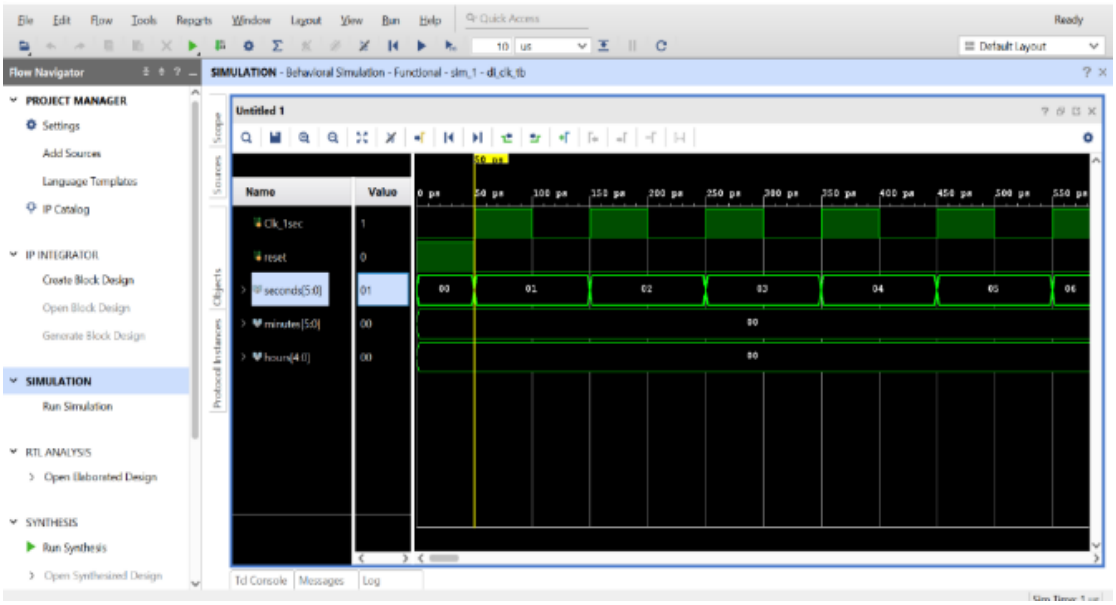

Fig. 5 Waveform for Seconds in Digital Clock

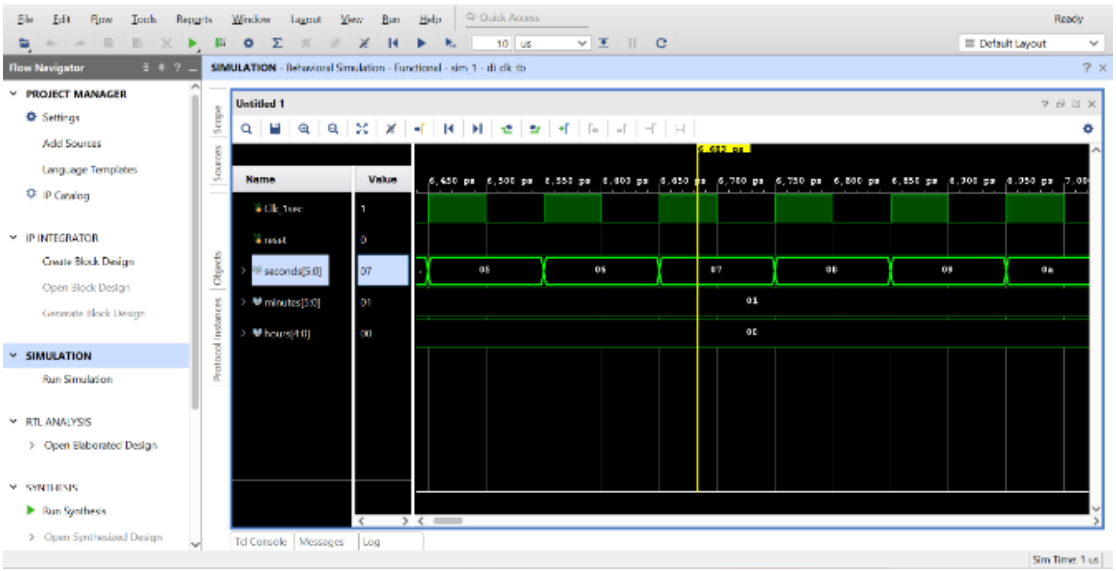

Fig. 6 Waveform for Minutes in Digital Clock

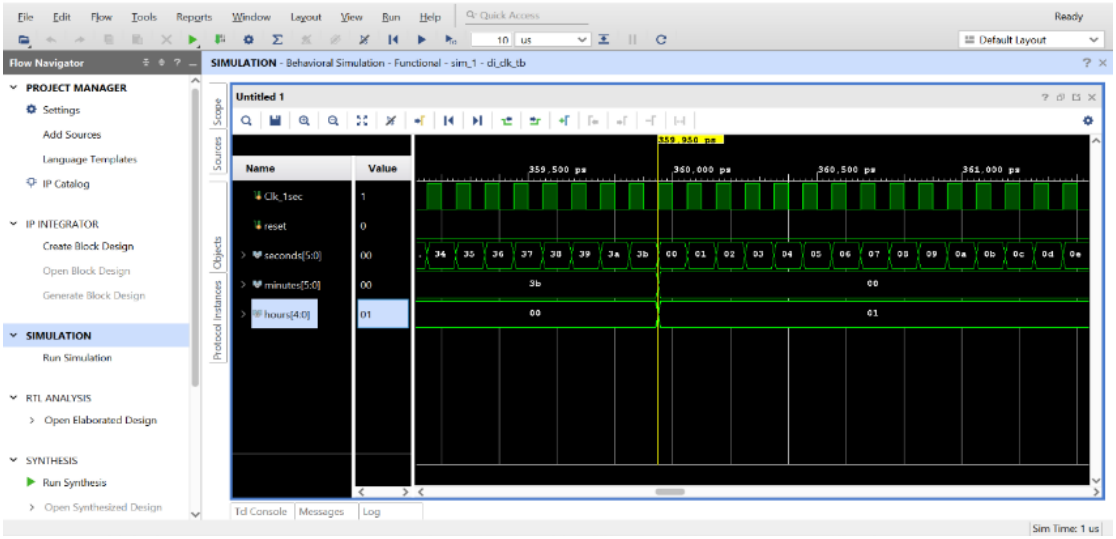

Fig. 7 Waveform for Hours in Digital Clock

V. CONCLUSION

Working with an FPGA board, allowed us to learn a lot and gain experience. To create a protocol for the interaction of a PMOD and an FPGA board, we learned how to connect both and work with them. Additionally, we gained a better understanding of the underlying ideas behind creating digital systems. Everyone in our group has made progress in several areas, including state machine comprehension, and building a structural data path for a digital system. Our project was a great opportunity to practice software and hardware co-design in a real-world setting, and this could be used frequently for experiments, sports, and other activities widely.

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