Power Reduction in Logic Gates using SAPON and LCNT techniques

[1]Ch. Suneetha, [2]M. Veena, [3]N. Anurag, [4]M. Tarun Reddy

[1]Associate professor, [2,3,4]Undergraduate student
Electronics and Communication Engineering,
Vignana Bharathi Institute of Technology, Hyderabad, India

***Abstract*- Logic gates serve as the efficient powerhouses of modern electronics, optimizing energy consumption and extending battery life in smartphones, laptops, and wearable devices. Two cutting-edge strategies methods, namely Leakage Control NMOS Transistor (LCNT) and Stackly Arranged low Power ON transistor (SAPON), are employed to enhance the power efficiency of the logic gates. The LCNT technique minimizes power consumption by increasing resistance along the path between the supply voltage (Vdd) and the ground (GND). On the other hand, SAPON prevents leakage current during the changeover stage, further reducing power consumption in the logic gate circuits. These circuits are implemented and analyzed using the Cadence tool with 45nm technology.**

***Index Terms*- Leakage Control NMOS Transistor (LCNT), Stackly Arranged low Power ON transistor (SAPON), Very Large-Scale Integration (VLSI).**

I. INTRODUCTION

The fundamental components of digital circuits are logic gates, enabling the creation of innovative technologies like smartphones, self-driving cars, and smart homes. Logic gates play a crucial role in various fields, from computer science and telecommunications to healthcare and aerospace, driving technological advancements and improving our daily lives.

In this paper, we analyzed power consumption in all basic logic gates and designed new logic gates using SAPON and LCNT techniques. We observed that average power consumption in logic gates is reduced when we integrated SAPON and LCNT techniques in it. More preferably SAPON showed the least power consumption compared to LCNT.

The format of the paper is as mentioned: Section II represents the literature survey and Section III gives an idea about power-consuming parameters. Section IV reflects the concept of logic gates while Section V says information regarding techniques used to reduce power consumption. Section VI depicts the analysis and outcomes of simulations performed with the Cadence tool. The work's conclusion is shown in Section VII.

II. LITERATURE SURVEY

Both NMOS and PMOS transistors are divided into two transistors in many logic circuits using this [1] approach. This paper uses [3] MTCMOS (Multi threshold CMOS) and Stack techniques and MTCMOS plus Stack are used for reducing leakage current below the threshold, which lessens power loss.A brand-new, cutting-edge method called LECTOR [4] has been developed for creating CMOS gates that consume significantly less power.

Sources Of Power Consumption

The Average power dissipation observed in VLSI Combined both s dynamic & static dissipation of power occurs in circuits.

Static Power Dissipation

The main causes of leakage power [5] are below the channel of threeshould permeability power & reverse bias P-N junctions current. Under threshold power

Dynamic Power Dissipation

A process of charging and discharging. The result is dynamic consumption due to the charging and discharge processes. Gives the formula for the interaction power usage [5].

$$P = \alpha * f * c * V_{dd}^2 \quad (1)$$

where, α - switching activity, f – frequency, C – load capacitance, V_{dd}^2 - supply voltage

Short-Circuit Power Dissipation

Leakage from short circuits has an enormous impact on dynamic power usage [5]. When the voltage required for the gates reaches a certain point during the transition, both the NMOS and PMOS voltage limitations are met, allowing both transistors to be turned on. Because of the characteristics of a CMOS architecture, power loss occurs when a straight conducting line created from the source of voltage to the ground is crossed while both transistors are turned on. This power depends on the I-V curve, the length, and the preference of the transistor loading capacitances.

$$I_d = I_s(e^{v/v_t} - 1) \quad (2)$$

III. LOGIC GATES

The fundamental parts are logic gates. The decisions that are made depend on the mix of digital signals that pass through logic gate designs in a circuit. There are 7 basic types of fundamental logic gates: OR, AND, XOR, or NOT to NOR, NAND, thereby and XNOR.

NOT Gate

A logic gate called a NOT gate only has one input and one output. The output it provides is the logical conclusion of the input.

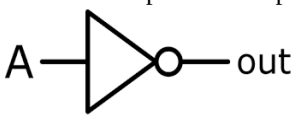

Fig. 1 NOT Gate

AND Gate

Logical conjunction (A) from mathematical logic is implemented by a simple digital logic gate. The AND gate only generates an output of HIGH (1) when all of its inputs are maximum.

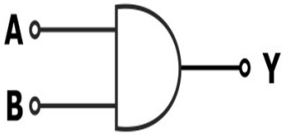

Fig. 2 AND Gate

OR Gate

The OR gate derives its name from the way it functions—which is like the logical inclusive "or"—which is how it operates. If one or both for the inputs are "true," the result will also be "true."

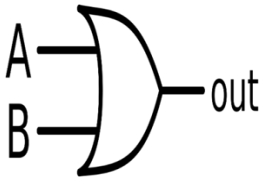

Fig. 3 OR Gate

NAND Gate

The output of a It is a logic gate called the NAND gate (NOT-AND gate) used in digital electronics, is opposite to that of an AND gate since it only gives a false output if all of its inputs are true.

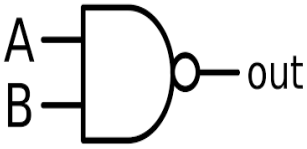

Fig. 4 NAND Gate

NOR Gate

Logical NOR being put into practice through the NOR gate, a digital logic gate. The output of the gate is LOW ((0)) if any or both of its inputs are HIGH (1) and LOW (0); otherwise, HIGH (1) is the output that is generated.

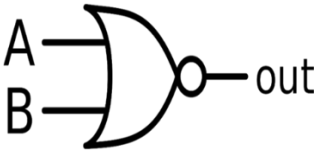

Fig. 5 NOR Gate

XOR Gate

An XOR gate, also referred to as an EOR, is a kind of digital logic gate. gate or an EXOR gate and spoken as if there are an odd number of valid inputs, exclusive OR produces a genuine output (1 or HIGH).

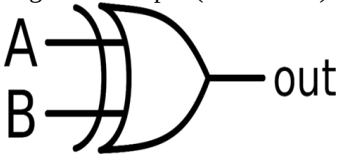

Fig. 6 XOR Gate

IV. PROPOSED TECHNIQUES

LCNT

The LCNT technique, as described in reference [6], is an approach aimed at reducing leakage current power. This technique involves the insertion of an addition of NMOS transistor after the pull-down section, as illustrated in Figure 7. By incorporating this extra NMOS transistor, the leakage power is effectively diminished. Notably, the added NMOS transistor functions as a self-controlled

element, eliminating the need for any additional inputs. The only requirement is to provide feedback from the output to the NMOS transistor.

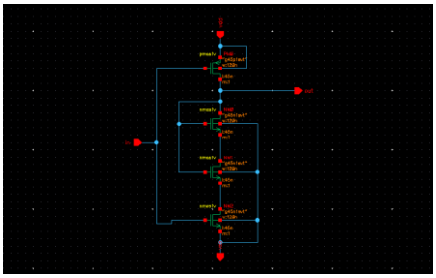

Fig.7 Schematic of LCNT NOT Gate

SAPON

In a particular technique described in reference [7], a method is employed to managethe use of two leakage-control transistors outside the logic circuitry to reduce the resistivity between the voltage supplied (Vdd) and the ground (GND). In order to avoid leakage current from an electrical short during the transition period, this setup was put in place. Additionally, Figure 8's representation of CMOS SAPON transistors, which are linked in series between Vdd and GND, is included in the technique. During the levelling phase, these transistors are responsible for managing a sub-threshold leakage current effectively.

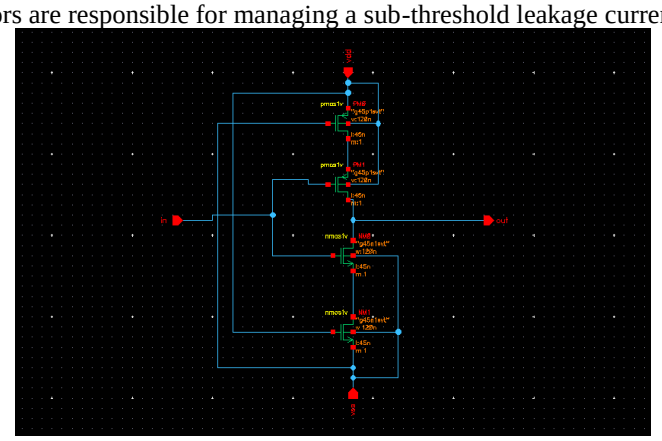

Fig.8 Schematic of SAPON NOT Gate

V. ANALYSIS AND RESULTS

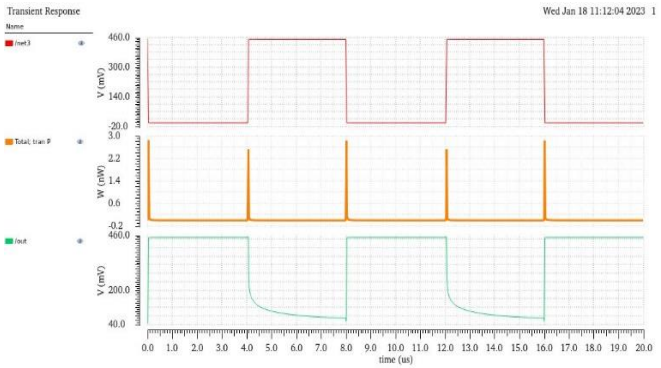

Fig. 9 Transient output of LCNT NOT Gate

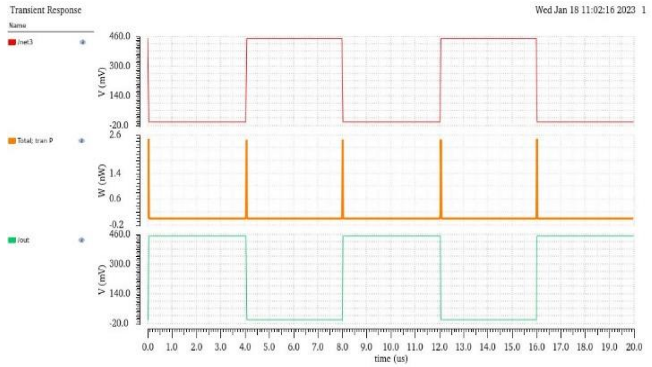

Fig. 10 Transient output of SAPON NOT Gate

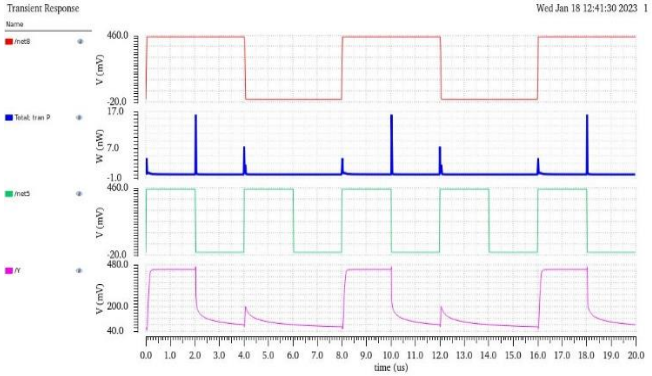

Fig. 11 Transient output of LCNT AND Gate

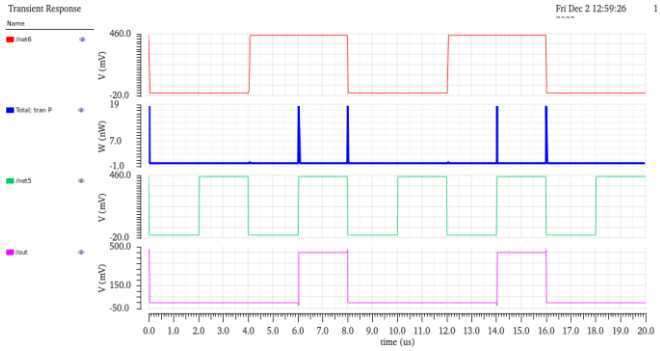

Fig. 12 Transient output of SAPON AND Gate

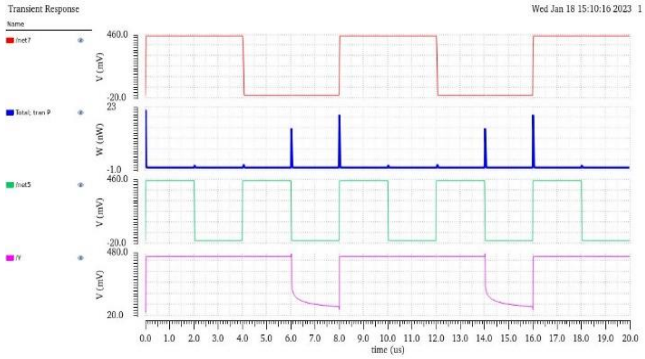

Fig. 13 Transient output of LCNT OR gate

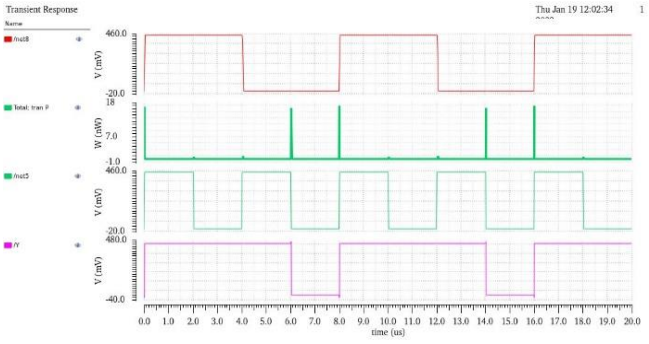

Fig. 14 Transient output of SAPON OR gate

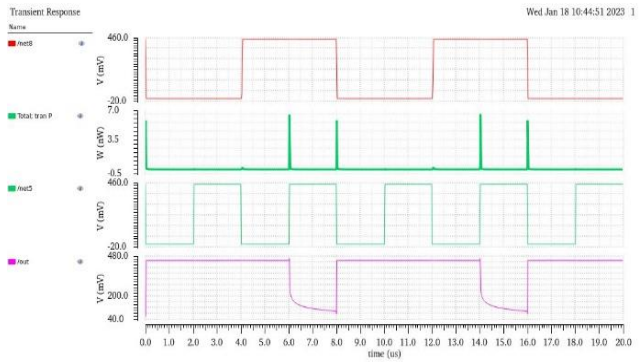

Fig. 15 Transient output of LCNT NAND gate

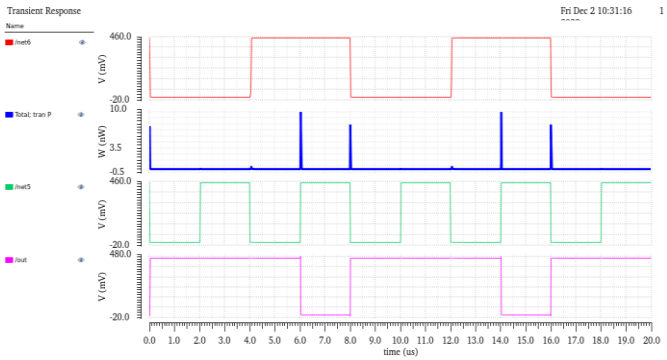

Fig. 16 Transient output of SAPON NAND gate

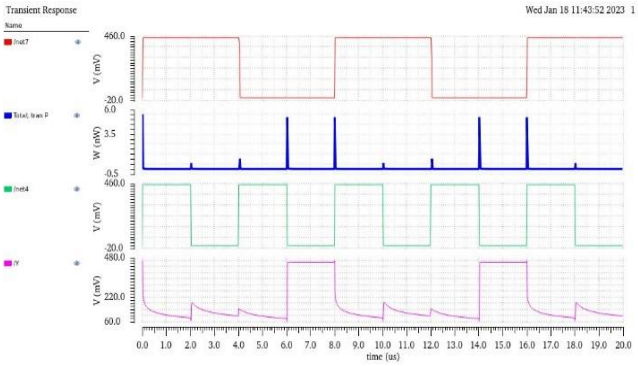

Fig. 17 Transient output of LCNT NOR gate

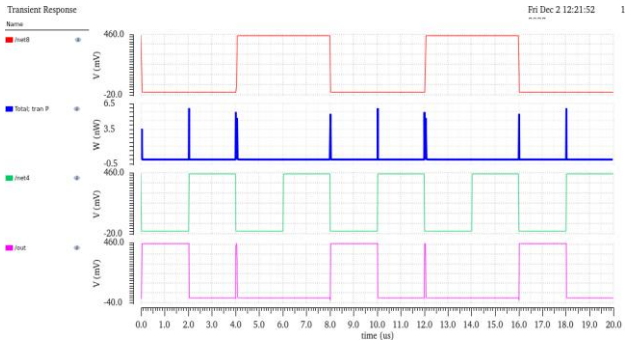

Fig. 18 Transient output of SAPON NOR gate

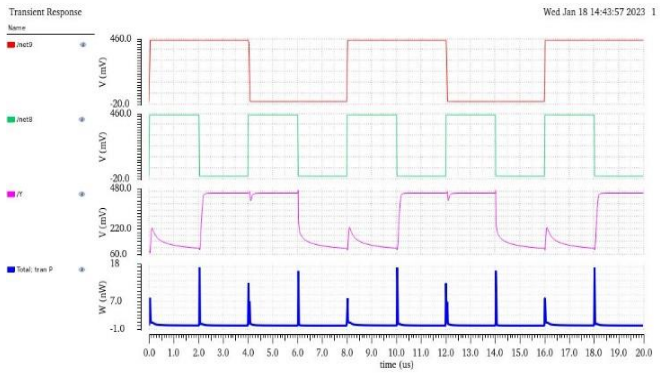

Fig. 19 Transient output of LCNT XOR gate

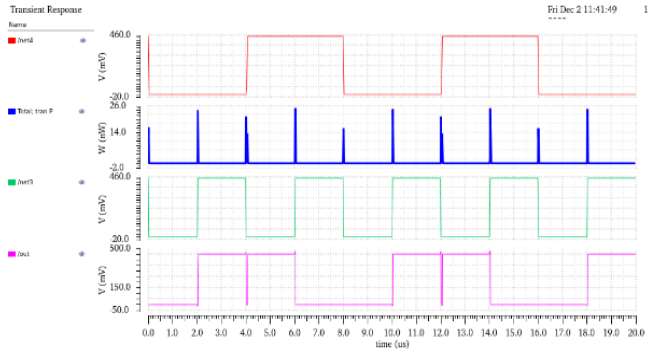

Fig. 20 Transient output of SAPON XOR gate

Table 1. Comparison of Power Consumption of all the basic gates using CMOS, LCNT and SAPON techniques

Logic Gates	CMOS	LCNT	SAPON
NOT	10.79E-12	10.31E-12	5.925E-12
AND	36.85E-12	50.76E-12	21.02E-12
OR	20.47E-12	24.71E-12	19.71E-12
NAND	19.33E-12	14.75E-12	11.80E-12
NOR	11.17E-12	14.23E-12	10.35E-12
XOR	109.6E-12	148.1E-12	68.15E-12

VI. CONCLUSION

In conclusion, the integration of LCNT and SAPON techniques emerges as a formidable solution to tackle the power consumption challenge in logic gates. LCNT effectively optimizes the power path, reducing energy wastage, while SAPON mitigates leakage current during critical transitions. These innovative techniques not only enhance power efficiency but also pave the way for sustainable and energy-conscious digital systems, ensuring a brighter future for technological advancements. The future scope for these techniques is reducing delay parameters.

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