

A review of surface potential of short channel MOSFETs in subthreshold regime

¹Swapnadip De, ²Angsuman Sarkar, ³Srijan Das

¹Associate Professor, ²Professor, ³Alumni
Department of Electronics and Communication Engineering,
Meghnad Saha Institute of Technology
Kolkata, India

Abstract- In this paper an analytical models of subthreshold surface potential for channel engineered and gate engineered MOSFETs are studied. The models are compared with simulation results from 2D DESSIS. It is seen that the results of the existing models tally with those from 2D DESSIS.

Index Terms- Surface potential, subthreshold, Gauss's law, channel engineering, gate engineering.

I. INTRODUCTION

The short channel effects can primarily be attributed to the reduction of the gate control over the channel. In the DMG MOSFET, the work function of the metal corresponding to gate1(M1) is greater than that for gate2(M2) and hence the threshold voltage corresponding to M1(V_{t1}) is greater than that corresponding to M2(V_{t2}). This has the inherent advantage of improved gate transport efficiency by modifying the electric field profile along the channel. Due to different work functions of two gates the surface potential profile is a step function, which ensures a reduction in the short channel effects and screening of the channel region under M1 from the drain potential variations. To reduce the short channel effects, the channel engineering approach like single halo(SH) also known as lateral asymmetric channel(LAC) or double halo(DH) implants are used. The channel engineering and the gate engineering techniques are combined to form novel device structures like Single halo Dual Material Gate and Double halo Dual Material gate MOSFETs have been proposed in this paper. Surface potential can be accurately predicted by solving the Poisson's equation along the entire channel region. This requires numerical solutions which are not suitable for use in circuit analysis as the solution does not contain finite number of terms in closed form and also the computation time requirement is high. Analytical models are used as an alternative to get solutions which are approximate but computationally efficient, so making it more convenient for understanding the device physics and handy for device design.

In a different approach called pseudo two-dimensional analysis Gauss's law is applied to a rectangular box covering the entire channel depletion region. Among the various methods of solving the Poisson's equation, this method produces a simpler manageable one-dimensional analytical expression retaining the two-dimensional accuracy to a greater extent. As the device dimension is reduced, the various leakage capacitances and the fringing capacitances at two ends of MOSFET play an important role in the expression of sub threshold surface potential. A simple expression for the parasitic inner fringing capacitance from the bottom edge of the gate electrode is considered and the charges induced in the source and the drain regions due to these capacitances are considered. The surface potential increases along the channel due to these charges. The models are verified with the 2D device simulator DESSIS. Very good agreements of our models with DESSIS are obtained.

II STUDY OF SURFACE POTENTIAL FOR SHORT CHANNEL MOSFETs

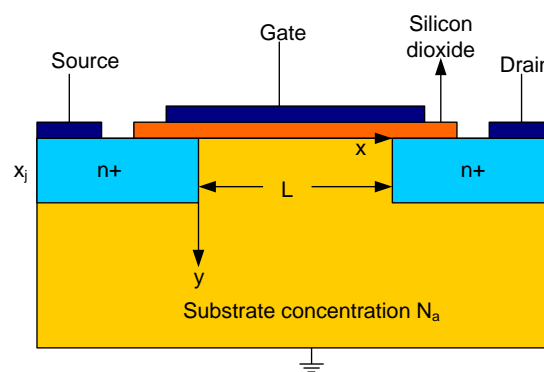


Fig 1: MOSFET structure

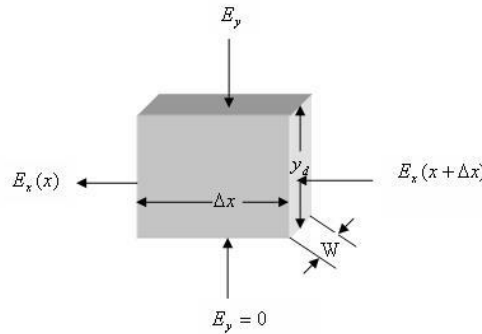


Fig 2:An elementary Gaussian surface in the channel covering the entire depletion region.

The MOSFET structure shown in Figure 1 is used to develop and implement the model. Applying Gauss law and neglecting mobile charge carriers to a rectangular box in the channel depletion region of the MOSFET shown in Figure 2, the following equation can be derived [1] :

$$\epsilon_{si} \frac{d^2 \psi_s}{dx^2} - \frac{C_{ox}}{Y_d} \psi_s = qN_a - \frac{C_{ox}}{Y_d} V'_{GS} \tag{1}$$

where $V'_{GS} = V_{GS} + V_{SB} - V'_{SB}$, $\psi_s(x)$ is the surface potential with respect to interior of the substrate bulk, V_{GS} is the gate-to-source voltage, V_{SB} is the source-to-body voltage, $V_{FB} = -0.56 - \phi_{fn} (N_a/n_i)$ is the flat-band voltage, t_{ox} is the gate oxide thickness, $C_{ox} = \epsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area, N_a is the channel doping density, Y_d is the depletion layer depth, and ϵ_{si} and ϵ_{ox} are the dielectric permittivities of Si and SiO_2 respectively.

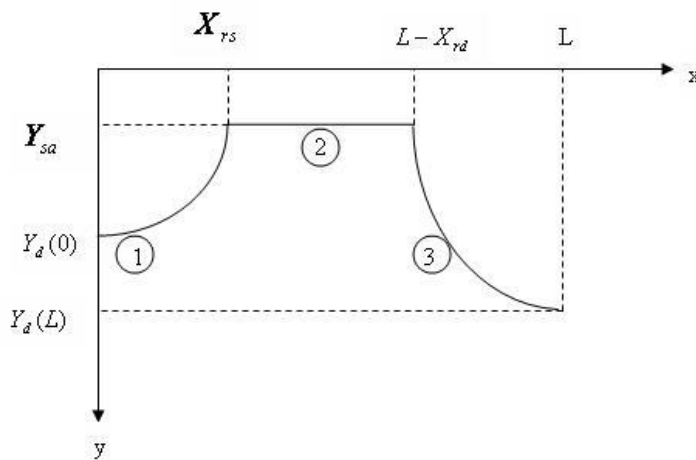


Fig 3 :Typical variation of depletion layer thickness in a long-channel MOS.

If the channel is sufficiently long, Fig 3, then the source-channel and the drain-channel junction depletion layers constitute a negligible portion of the entire channel length, and the surface potential profile over the channel outside the junction depletion layers is sufficient to compute any quantity which depends on it. With this consideration, when the device is in the weak inversion, the surface potential profile may be considered to remain constant at $\psi_{sa} = \left(-\gamma/2 + \sqrt{\gamma^2/4 + V_{GB} - V_{FB}} \right)^2$ and is dependent only on the gate-to-body bias V_{GB} , where $\gamma = \sqrt{2q\epsilon_{si}N_a/C_{ox}}$ is the body effect coefficient and $\phi_t = kT/q$ is the thermal voltage. However, for short-channel MOSFETs, the contribution of the two junction regions is no longer negligible and the so called charge sharing effect has to be taken into account for any modeling work [1,2,3,4,5]. It is clear from (1) that the surface potential at a point depends on the depletion layer thickness which is not constant. As such, it is required that $Y_d(x)$ be modeled first for an accurate prediction of the surface potential.

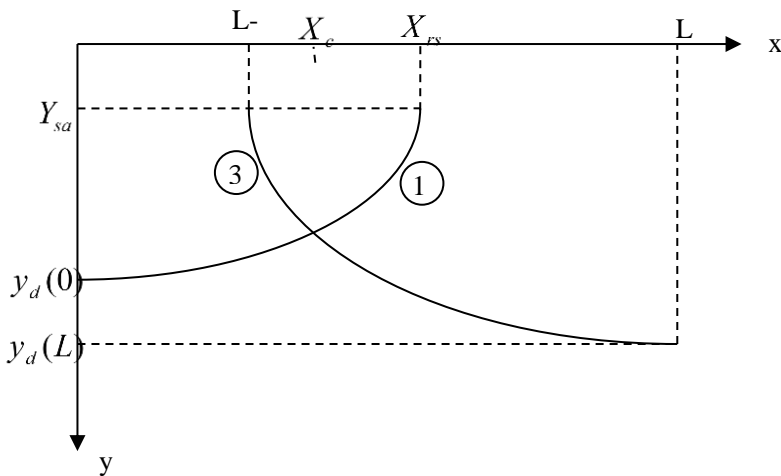


Fig 4: Typical variation of depletion layer thickness in a short-channel MOS.

Unfortunately, the depletion layer depth around the source and drain junctions is a complex function of substrate doping, gate and source/drain bias voltages. A good model should not only have a physically based approximate and simple description for it but this should give an analytical solution of (1) also. A good model must take into account the Fringing effect also for perfect estimation of surface potential. We give a brief account of the Fringing capacitances first and then introduce the Fringing potential due to inner fringing capacitance in the model [4,5].

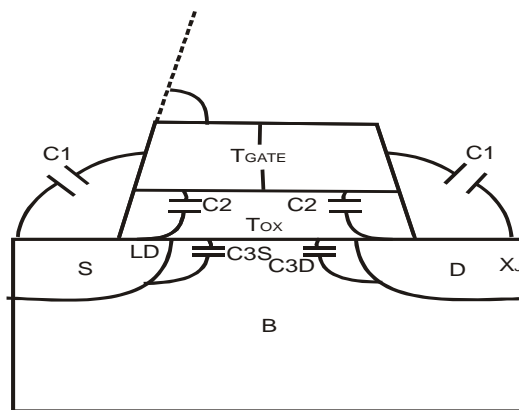


Fig 5 Fringing Capacitance Components C1, C2, and C3.

Here C1 is the outer-fringing-field capacitance between gate and source or drain electrode. C2 is the direct overlap capacitance between gate and source or drain junction. C3 is the inner-fringing-field capacitance between gate and the side wall of the source or drain junction. C3 becomes nonzero when the channel is depleted of mobile carriers and so some electric fields originating from the gate are terminated at the side wall of source or drain junction.

For C1, C2, and C3, we followed the equations:

$$C1 = W \cdot \frac{\epsilon_{ox}}{\alpha} - \log_e \left(1 + \frac{T_{GATE}}{T_{ox}} \right) \tag{2}$$

$$C2 = W \cdot \frac{\epsilon_{ox}}{T_{ox}} (LD + 0.5 T_{ox}) \left(\frac{1 - \cos \alpha}{\sin \alpha} + \frac{\cos \delta}{\sin \delta} \right) \tag{3}$$

$$\text{where } \delta = 0.5 \psi \cdot \frac{\epsilon_{ox}}{\epsilon_s} \tag{4}$$

where α is the slanting angle of gate electrode in radians. T_{GATE} is the thickness of the gate electrode. W is the channel width, and LD is the metallurgical lateral diffusion of source, drain junction as shown in Fig5. ϵ_{ox} and ϵ_0 are the dielectric constants of oxide and silicon, respectively. C_F is the maximum value of the inner-fringing capacitance component C3.

$$C_F = W \cdot \frac{\epsilon_{ox}}{\delta} \cdot \log_e \left(1 + \frac{x_j \sin \alpha}{T_{OX}} \right) \quad (5)$$

where x_j is the depth of the source, drain junctions. The capacitance components $C1$ and $C2$ are bias-independent and they are added to gate-drain or gate-source overlap capacitances, C_{GDO} and C_{GSO} . The capacitance component $C3$ is bias-dependent and it is modeled as a charge based form. Hence:

$$Q_{D,F} = -C_F \cdot \frac{V_{DS} - V_{DS}}{1 + \exp\left(-\frac{V_{GB} - V_{FB}}{30\phi_t}\right)} = V_{fs} \quad (6)$$

$$Q_{S,F} = -C_F \cdot \frac{V_{GST} - V_{GS} + V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F - V_{BS}}}{1 + \exp\left(-\frac{V_{GB} - V_{FB}}{30\phi_t}\right)} = V_{fd} \quad (7)$$

V_{DS} is obtained as given below.

The surface potential at the source end, Ψ_{SO} , is computed using the algorithm for $V_{CB} = V_{SB}$. The surface potential at the drain end, Ψ_{SL} , is computed from V_{DS} and V_{DSSAT} , where V_{DS} is the applied drain-to-source voltage and V_{DSSAT} is the drain saturation voltage. Hence Ψ_{SL} can be written as

$$\Psi_{SL} = \Psi_{SO} + V_{DS} \quad (8)$$

where $V_{DS} = V_{DS}$ is the linear region and $V_{DS} = V_{DSSAT}$ is the saturation region. To make the smooth transition for V_{DS} between linear and saturation regions, a smooth function which we call "saturation function," S , is derived as

$$S(z) = 1 - \frac{\log_e(1 + e^{A(1-z)})}{\log_e(1 + e^A)} \quad (9)$$

Where z is V_{DS}/V_{DSSAT} . Large A gives a steep transition between the linear and saturation regions and small A gives a smooth transition. This parameter A is set to be a model parameter in the implementation. However, the computation of (3.9) is costly in computer time because it includes time consuming exponential and logarithmic functions. For the computational efficiency, another cubic spline function $SF()$ is derived from (9). The saturation function is computed only once in the SPICE setup stage to compute the cubic spline coefficients of $SF()$, and $SF()$ is repeatedly used for the model computation.

Hence, the effective drain to source voltage V_{DS} is computed from

$$V_{DS} = SF\left(\frac{V_{DS}}{V_{DSSAT}}\right) \cdot (V_{DSSAT} - V_{DSSAT,0}) \quad \text{where } V_{DSSAT,0} \text{ is } V_{DSSAT} \text{ at } V_{GST} = 0.$$

$Q_{D,F}$ is added to the drain charge Q_D , $Q_{S,F}$ is added to the source charge Q_S and $-(Q_{D,F} + Q_{S,F})$ is added to Q_G . The exponential term in (6) and (7) is added to guarantee that the channel-side-fringing-field capacitance is 0 in the accumulation region. Conceptually, the nominator in (6) is 0 in the linear region and it is linearly dependent on $(V_{DS} - V_{DSSAT})$ in the saturation region. Similarly, the nominator in (7) is 0 when $V_{GS} > V_{TH}$ and it is proportional to $(-V_{GS} + V_{TH})$ when $V_{GS} < V_{TH}$. The constant 30 in (6) and (7) is a heuristic factor to determine the slope of the transition.

Keeping these requirements in mind and also considering the typical variation of $Y_d(x)$ with x as shown in Fig 4, we propose an empirical model for this as $Y_d(x) = (ax + b)^2$ with the source and drain end values $Y_d(0) = X_j + \sqrt{2\epsilon_{si}(V_{SB} + V_{bi} + V_{fs})/(qN_a)} = X_j + X_{rs}$, where V_{fs} is the inner fringing potential in source end and $X_j + \sqrt{2\epsilon_{si}(V_{SB} + V_{bi} + V_{fd})/(qN_a)} = X_j + X_{rd}$ respectively, where X_j is the junction depth, V_{fd} is the inner fringing potential in drain end, $X_{rs} = \sqrt{2\epsilon_{si}(V_{SB} + V_{bi} + V_{fs})/(qN_a)}$ and $X_{rd} = \sqrt{2\epsilon_{si}(V_{DB} + V_{bi} + V_{fd})/(qN_a)}$ are the depth of penetrations of the depletion layers into the channel / substrate due to the built-in potential V_{bi} (between the n^+ -source/drain and the p-type channel/substrate) and the reverse bias V_{SB} and V_{DB} at the source and drain ends respectively, $V_{DB} = V_{DS} + V_{SB}$ is the drain-to-body bias, L is the effective channel length defined as the distance from the edge of the source to the edge of the drain as shown in Figure 4. At the source end, $Y_d(0) = X_j + X_{rs}$ and as one moves toward the drain end it decreases to $Y_{sa} = \sqrt{2\epsilon_{si}\psi_{sa}/(qN_a)}$ at the point where $x = X_{rs}$ (curve 1) following this second order relation. Similarly, at the drain end, $Y_d(L) = X_j + X_{rd}$ and as one moves toward the source end it decreases to Y_{sa} at the point where $x = L - X_{rd}$ (curve 3) following a similar relation. In general, the channel may

be divided into three regions with the depletion layer thickness modeled as $Y_d(x) = (ax + b)^2$ with known values at the two ends in all the three regions.

In reality, in the vicinity of the two ends of the channel, a significant portion of the field lines emanating from source/drain are mapped onto the space charges below the source/drain (outside the Gaussian box in the channel) and hence a reduced value of the contribution to the surface integration (Gauss' law) by the two side walls needs to be considered. However, as we move away from the two ends, this effect diminishes and finally, for a typical long-channel device, it reduces to zero where $Y_d(x) = Y_{sa}$ (central portion of the channel) [4,5]. In our analysis, this variation is modeled by considering a reduced value of the height of the side walls at the two ends $Y_d(x)$ and $Y_d(L)$. Further, this effect becomes more prominent for higher source/drain bias. The best fit of the model surface potential profile with ISE TCAD is found for the bias dependent fitting parameter $\zeta_s = 2(V_{SB} + V_{bi}) / V_{bi}$ for the source side and $\zeta_d = 2(V_{DB} + V_{bi}) / V_{bi}$ for the drain side. In other words, while computing a and b we use $Y_d(o) / \zeta_s$ and $Y_d(L) / \zeta_d$, instead of, $Y_d(0)$ and $Y_d(L)$ respectively. Note that such a function for the fitting parameter is logical in the sense that it is dimensionally correct and also when $V_{SB} = V_{DB}$, exactly a symmetrical surface potential profile between the source and drain is produced. This fitting parameter takes into account other fringing effects and leakage capacitances at the source and drain end.

Using $Y_d(x) = (ax + b)^2$ in (1) we get

$$(ax + b)^2 \frac{d^2 \psi_s}{dx^2} - \frac{C_{ox}}{\epsilon_{si}} \psi_s = \frac{qNa}{\epsilon_{si}} (ax + b)^2 - \frac{C_{ox}}{\epsilon_{si}} V'_{GS} \quad (10)$$

The complete solution of (10) is given by

$$\begin{aligned} \psi_s(t) = & \frac{1}{\sinh(dt'' - dt')} \{ (\psi'' - V'_{GS} - \beta e^{2t''}) \\ & \times e^{1/2(t-t'')} \sinh(dt - dt') \\ & - (\psi' - V'_{GS} - \beta e^{2t'}) e^{\frac{1}{2}(t-t')} \sinh(dt - dt'') \} \\ & + \beta e^{2t} + V'_{GS} \end{aligned} \quad (11)$$

where t is a substituted parameter defined as $t = \ln(ax + b)$, t' and t'' are the two end values of the parameter t in the given region, $d = \sqrt{(1/2)^2 + C_{ox} / (\epsilon_{si} a^2)}$, $\beta = qN_a / (2\epsilon_{si} a^2 - C_{ox})$ and $\psi_s(t)|_{t=t'} = \psi'$, $\psi_s(t)|_{t=t''} = \psi''$ are the boundary conditions.

Differentiation of (11) gives

$$\begin{aligned} \frac{d\psi_s}{dx} = & \frac{(\psi'' - V'_{GS} - \beta e^{2t'}) e^{\frac{1}{2}(t+t')}}{\sinh(dt'' - dt')} \{ d a \cosh(dt - dt'') \} \\ & \times \{ d a \cosh(dt - dt') + 1/2 a \sinh(dt - dt') \} \\ & - \frac{(\psi' - V'_{GS} - \beta e^{2t'}) e^{-1/2(t+t'')}}{\sinh(dt'' - dt')} \{ d a \cosh(dt - dt'') \} \\ & + \frac{1}{2} a \sinh(dt - dt'') \} + 2a\beta e^t \end{aligned} \quad (12)$$

As mentioned earlier, the channel in general, is required to be divided into three regions with three different sets of parameters a and b . However, at any point over the channel, the surface potential and its derivative are continuous. Based on the channel length, doping concentration and applied potentials, following two cases for the three regions are required to be considered.

Case-1 : $X_{rs} \leq L - X_{rd}$: This case arises when the channel is sufficiently long.

Region-I : $x_1 = 0 < x \leq x_2 = X_{rs}$: The corresponding values of y are $y_1 = \{ X_j + \sqrt{2\epsilon_{si} V_1 / (qN_a)} \} / \zeta_s$ and $y_2 = Y_{sa}$. The end potentials are $V_1 = V_{bi} + V_{SB}$ and V_2 to be evaluated.

Region-II : $x_2 \leq x < x_3 = L - X_{rd}$: Here the depletion layer thickness is constant and equal to Y_{sa} . The end potentials V_2 and V_3 at both the ends are to be evaluated.

Region-III : $x_3 < x \leq x_4 = L$: The corresponding y values are $y_3 = Y_{sa}$ and $y_4 = \{ X_j + \sqrt{2\epsilon_{si} V_4 / (qN_a)} \} / \zeta_d$. The end potentials are V_3 to be evaluated and $V_4 = V_{bi} + V_{DB}$.

Case-2 : $X_{rs} > L - X_{rd}$: In general, this case arises when the source and the drain regions are close to each other. The tips of the two depletion layers (curve 1 and 3) due to source and drain cross each other and the DIBL comes into effect. The crossing point is simply obtained by equating the two corresponding equations as $x_c = (b_3 - b_1) / (a_1 - a_3)$, where the parameters (a_1, b_1) and (a_3, b_3)

correspond to the curve 1 and 3 respectively. It is assumed that upto $x = x_c$ the depletion layer thickness is controlled by the source side and beyond this it is affected by the drain side and nowhere in the channel the thickness is constant in contrast to the long-channel devices. This is nothing but short channel effect. To enable the use of the same set of solutions as in long channel case, we divide the channel into three regions for this case as well. This is done by either dividing the first part (0 to x_c) or second part (x_c to L) arbitrarily into two regions. In our analysis we have divided the first part into two regions as follows :

Region-I : $x_1 = 0 < x \leq x_2 = x_c / 2$: The corresponding y values are $y_1 = \left\{ X_j + \sqrt{2\epsilon_{si} V_1 / (qN_a)} \right\} / \zeta_s$ and $y_2 = Y_{sa}$ with the end potentials $V_1 = V_{bi} + V_{SB} + V_{fs}$ and V_2 to be evaluated.

Region-II : $x_2 < x \leq x_3 = x_c$: The corresponding y and the end potential values are same as in region-I.

Region-III : $x_3 < x \leq x_4 = L$: The corresponding y values are $y_3 = Y_{sa}$ and $y_4 = \left\{ X_j + \sqrt{2\epsilon_{si} V_4 / (qN_a)} \right\} / \zeta_d$ with the end potentials V_3 to be evaluated and $V_4 = V_{bi} + V_{DB} + V_{fd}$.

The complete solution needs to be obtained in all the three regions. However, it may be noted that, if in a region $Y_d(x) = Y_0$ is constant, the corresponding parameters are $a=0$ and $b = \sqrt{Y_0}$. But then, $d = \sqrt{(1/2)^2 + C_{ox} / (\epsilon_{si} a^2)}$ becomes indeterminate. Such a situation is handled by considering the limiting values of the following product terms :

$$da = \sqrt{C_{ox} / \epsilon_{si}} \text{ and } dt = (x/b) \sqrt{C_{ox} / \epsilon_{si}}$$

The general division of the channel into the following three regions leads to the values of the various parameters, boundary values and ψ_s as

Region-I: $x_1 < x \leq x_2 (\equiv t_1 < t \leq t_2)$, $a = a_1, b = b_1, d = d_1, \beta = \beta_1, \psi' = V_1, \psi'' = V_2$

$$\begin{aligned} \psi_s(t) = & \frac{1}{\sinh(d_1 t_2 - d_1 t_1)} \left\{ (V_2 - V'_{GS} - \beta_1 e^{2t_2}) \right. \\ & \times e^{1/2(t-t_2)} \sinh(d_1 t - d_1 t_1) \\ & - (V_1 - V'_{GS} - \beta_1 e^{2t_1}) e^{\frac{1}{2}(t-t_1)} \\ & \left. \times \sinh(d_1 t - d_1 t_2) \right\} + \beta_1 e^{2t} + V'_{GS} \end{aligned} \tag{13}$$

Region-II : $x_2 < x \leq x_3 (\equiv t_3 < t \leq t_4)$, $a = a_2, b = b_2, d = d_2, \beta = \beta_2, \psi' = V_3, \psi'' = V_3$

$$\begin{aligned} \psi_s(t) = & \frac{1}{\sinh(d_2 t_4 - d_2 t_3)} \left\{ (V_3 - V'_{GS} - \beta_2 e^{2t_4}) \right. \\ & \times e^{1/2(t-t_4)} \sinh(d_2 t - d_2 t_3) \\ & - (V_2 - V'_{GS} - \beta_2 e^{2t_3}) e^{\frac{1}{2}(t-t_3)} \\ & \left. \times \sinh(d_2 t - d_2 t_4) \right\} + \beta_2 e^{2t} + V'_{GS} \end{aligned} \tag{14}$$

Region-III : $x_3 < x \leq x_4 (\equiv t_5 < t \leq t_6)$, $a = a_3, b = b_3, d = d_3, \beta = \beta_3, \psi' = V_3, \psi'' = V_4$

$$\begin{aligned} \psi_s(t) = & \frac{1}{\sinh(d_3 t_6 - d_3 t_5)} \left\{ (V_4 - V'_{GS} - \beta_3 e^{2t_6}) \times e^{1/2(t-t_6)} \sinh(d_3 t - d_3 t_5) \right. \\ & \left. (V_3 - V'_{GS} - \beta_3 e^{2t_5}) e^{\frac{1}{2}(t-t_5)} \times \sinh(d_3 t - d_3 t_6) \right\} + \beta_3 e^{2t} + V'_{GS} \end{aligned} \tag{15}$$

Using (12) and applying the continuity of derivative of the potentials at the interface between the region-I and the region-II we get

$$a_{11} V_2 + a_{12} V_3 = A_1 \tag{16}$$

where $a_{11} = (d_1 a_1 \coth(d_1 t_2 - d_1 t_1) + (1/2) a_1) e^{-t_2} + (d_2 a_2 \coth(d_2 t_4 - d_2 t_3) - (1/2) a_2) e^{-t_3}$

and $A_1 = -(V'_{GS} + \beta_2 e^{2t_4}) \operatorname{cosech}(d_2 t_4 - d_2 t_3) d_2 a_2 e^{\frac{1}{2}(t_3+t_4)}$

$$\begin{aligned}
 &+ (V'_{GS} + \beta_2 e^{2t_3}) \left(d_2 a_2 \coth(d_2 t_4 - d_2 t_3) - \frac{1}{2} a_2 \right) e^{-t_2} \\
 &+ (V'_{GS} + \beta_1 e^{2t_2}) \left(d_1 a_1 \coth(d_1 t_2 - d_1 t_1) + \frac{1}{2} a_1 \right) e^{-t_2} \\
 &+ (V_1 - V'_{GS} - \beta_1 e^{2t_1}) \operatorname{cosech}(d_1 t_2 - d_1 t_1) d_1 a_1 \\
 &\times e^{-\frac{1}{2}(t_2+t_1)} + 2a_2 \beta_2 e^{t_3} - 2a_1 \beta_1 e^{t_2}
 \end{aligned} \tag{17}$$

Similar application of the boundary conditions at the interface between the region-II and the region-III gives $a_{21}V_2 + a_{22}V_3 = A_2$ (18)

where $a_{21} = -\operatorname{cosech}(d_2 t_4 - d_2 t_3) d_2 a_2 e^{-\frac{1}{2}(t_4+t_3)}$ (19)

$$\begin{aligned}
 a_{22} = &(d_2 a_2 \coth(d_2 t_4 - d_2 t_3) + (1/2) a_2) e^{-t_4} \\
 &+ (d_3 a_3 \coth(d_3 t_6 - d_3 t_5) - (1/2) a_3) e^{-t_5} \text{ and}
 \end{aligned} \tag{20}$$

$$\begin{aligned}
 A_2 = &(V_4 - V'_{GS} - \beta_3 e^{2t_6}) \operatorname{cosech}(d_3 t_6 - d_3 t_5) d_3 a_3 e^{-\frac{1}{2}(t_5+t_6)} \\
 &+ (V'_{GS} + \beta_3 e^{2t_5}) \left(d_3 a_3 \coth(d_3 t_6 - d_3 t_5) - \frac{1}{2} a_3 \right) e^{-t_5} \\
 &+ (V'_{GS} + \beta_2 e^{2t_4}) \left(d_2 a_2 \coth(d_2 t_4 - d_2 t_3) + \frac{1}{2} a_2 \right) e^{-t_4} \\
 &- (V'_{GS} + \beta_2 e^{2t_3}) \operatorname{cosech}(d_2 t_4 - d_2 t_3) d_2 a_2 \\
 &\times e^{-\frac{1}{2}(t_4+t_3)} + 2a_3 \beta_3 e^{t_5} - 2a_2 \beta_2 e^{t_4}
 \end{aligned} \tag{21}$$

Solving (16) and (18) using Cramer's rule

$$V_2 = \frac{\begin{vmatrix} A_1 & a_{12} \\ A_2 & a_{22} \end{vmatrix}}{\begin{vmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{vmatrix}} \text{ and } V_3 = \frac{\begin{vmatrix} a_{11} & A_1 \\ a_{21} & A_2 \end{vmatrix}}{\begin{vmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{vmatrix}} \tag{22}$$

Substituting the values of V_2 and V_3 from (22), ψ_s in all the three regions may easily be computed.

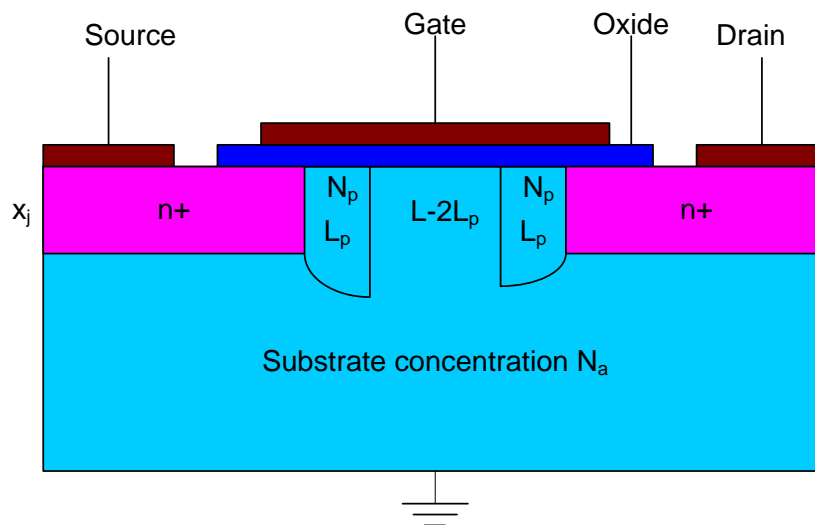


Fig 6 The n-channel DH transistor structure and doping profile.

The structure of an n-channel double halo (DH), also known as pocket-implanted MOS transistor, with n^+ -polysilicon gate is shown in Fig6. In this case there are two pocket regions with a higher doping concentration N_p at the two ends of the channel placed

symmetrically upto a distance of L_p , while a relatively lower concentration N_a in the middle portion of length $L - 2L_p = L_a$ are used. The model incorporates the variation of the depletion layer due to such pocket doping in addition to the applied voltages.

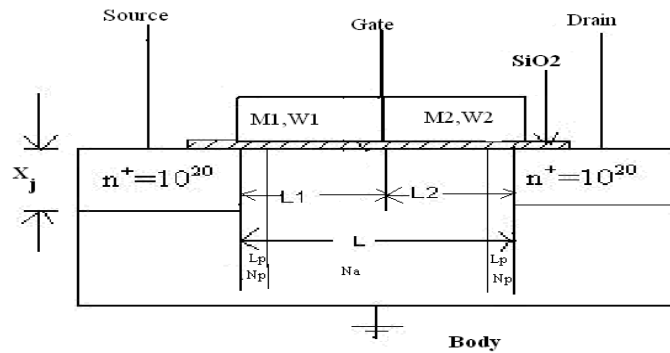


Fig 7An n-channel Double halo DMG MOSFET structure.

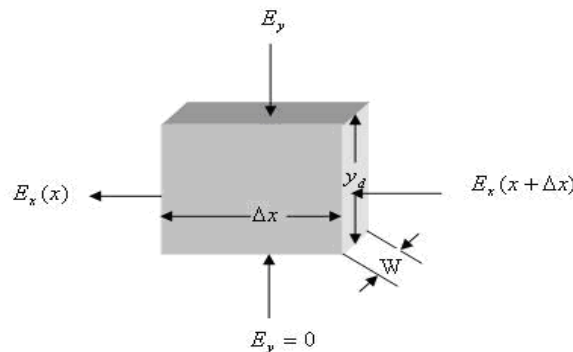


Fig 8A rectangular Gaussian Box in the entire depletion region.

An n-channel Double halo DMG MOSFET structure is shown in Fig 7. By applying Gauss’s law to the box shown in Figure 8 and neglecting the inversion layer charges in the channel depletion region, a pseudo-2D Poisson’s equation can be obtained as follows:

$$\epsilon_{si} \frac{d^2 \psi_s}{dx^2} - \frac{C_{ox}}{Y_d} \psi_s = qN_a - \frac{C_{ox}}{Y_d} V_{GS} \tag{39}$$

where $V'_{GS} = V_{GS} + V_{SB} - V'_{SB}$, $\psi_s(x)$ is the surface potential with respect to interior of the substrate bulk, V_{GS} is the gate-to-source voltage, V_{SB} is the source-to-body voltage, $V_{FB} = -0.56 - \phi_{fn} (N_a/n_i)$ is the flat-band voltage, t_{ox} is the gate oxide thickness, $C_{ox} = \epsilon_{ox}/t_{ox}$ is the oxide capacitance per unit area, N_a is the channel doping density, Y_d is the depletion layer depth, and ϵ_{si} and ϵ_{ox} are the dielectric permittivities of Si and SiO₂ respectively [1,2,12].

The flat-band voltages for the gate metals are given by

$$V_{FB1} = (W_1 - W_{si})/q. \tag{40}$$

$$V_{FB2} = (W_2 - W_{si})/q. \tag{41}$$

where W_1 and W_2 are the work functions of the gate metals and W_{si} that of the silicon substrate respectively. It is considered that $W_1 > W_2$.

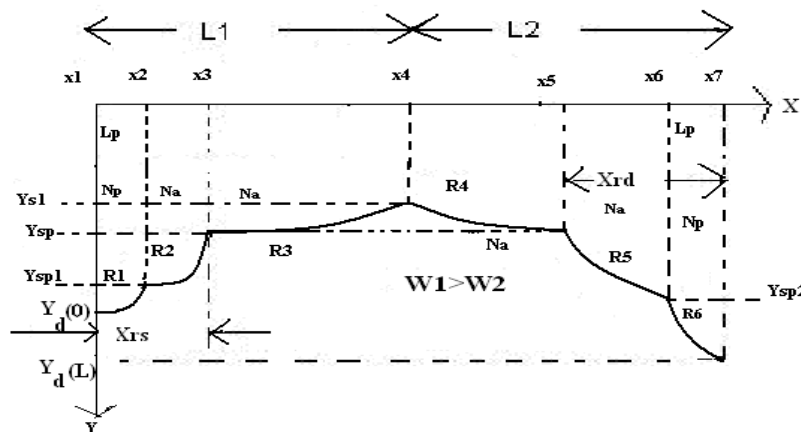


Fig 9Typical variation of the depletion layer depth $Y_d(x)$.

The typical variation of depletion layer depth for the Double halo Dual Material Gate MOSFET is shown in Figure 9.

The fringing capacitances originate from the portion of the field lines originating from the gate electrode and terminating on the drain and source junctions. For long channel MOSFET the inner fringing capacitance effects are negligible but for short channel devices their contributions are considerable. For the subthreshold surface potential estimation the inversion layer is assumed to be negligible and as a result the horizontal field components of the electric field from the drain is assumed to be constant. The fringing capacitance in the absence of an inversion layer charge is constant and is approximately given by [4,5],

$$C_f = \frac{2\epsilon_{si}W}{\pi} \ln \left[1 + \frac{X_j}{t_{ox}} \operatorname{Sim} \left(\frac{\pi \epsilon_{ox}}{2 \epsilon_{si}} \right) \right] \tag{42}$$

Where ϵ_{ox} and ϵ_{si} are the dielectric constants of oxide and silicon, respectively, W is the channel width, L is the effective channel length, t_{ox} is the oxide thickness and X_j is the depth of the source and the drain junctions. For example the contribution of the fringing capacitance C_f to the gate-to-drain capacitance C_{gd} is represented by [4,5],

$$C_{gdf} = C_f \left(1 - \frac{2C_{gd}}{C_0} \right) \tag{43}$$

$$C_0 = WL \frac{\epsilon_{ox}}{t_{ox}} \tag{44}$$

Where C_0 is the total gate-to-oxide capacitance. The use of equation (39) satisfies the boundary conditions for $V_D=0$ where $V_D=$ Drain voltage. For $V_D=0$, $C_{gd}=0.5C_0$ and hence $C_{gdf}=0$

The vanishing of fringing capacitance in the linear region is the result of the high carrier concentration in the channel which isolates the drain junction from the filed lines originating from the gate electrode. The fringing and the overlap potential as a result of this capacitance at the source and the drain end are calculated using Coulomb's law.

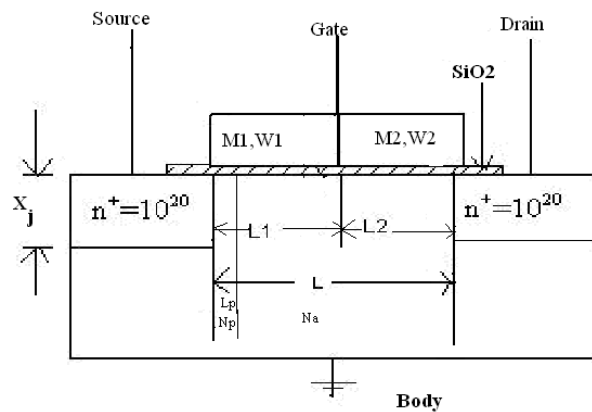


Fig 10 The structure of the n-channel single halo DMG MOSFET transistor.

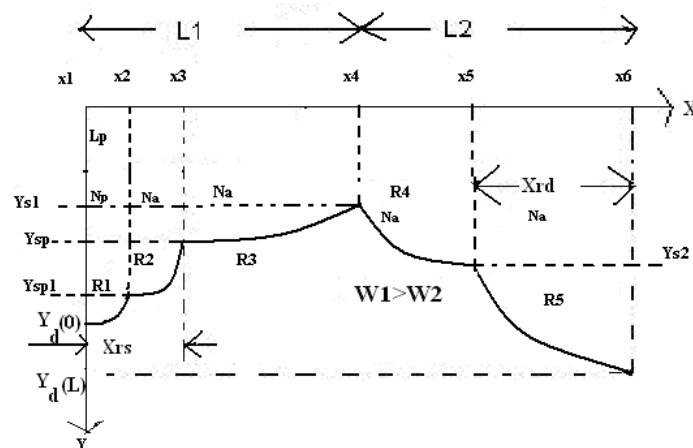


Fig 11 Typical variation of the depletion layer depth $Y_d(x)$.

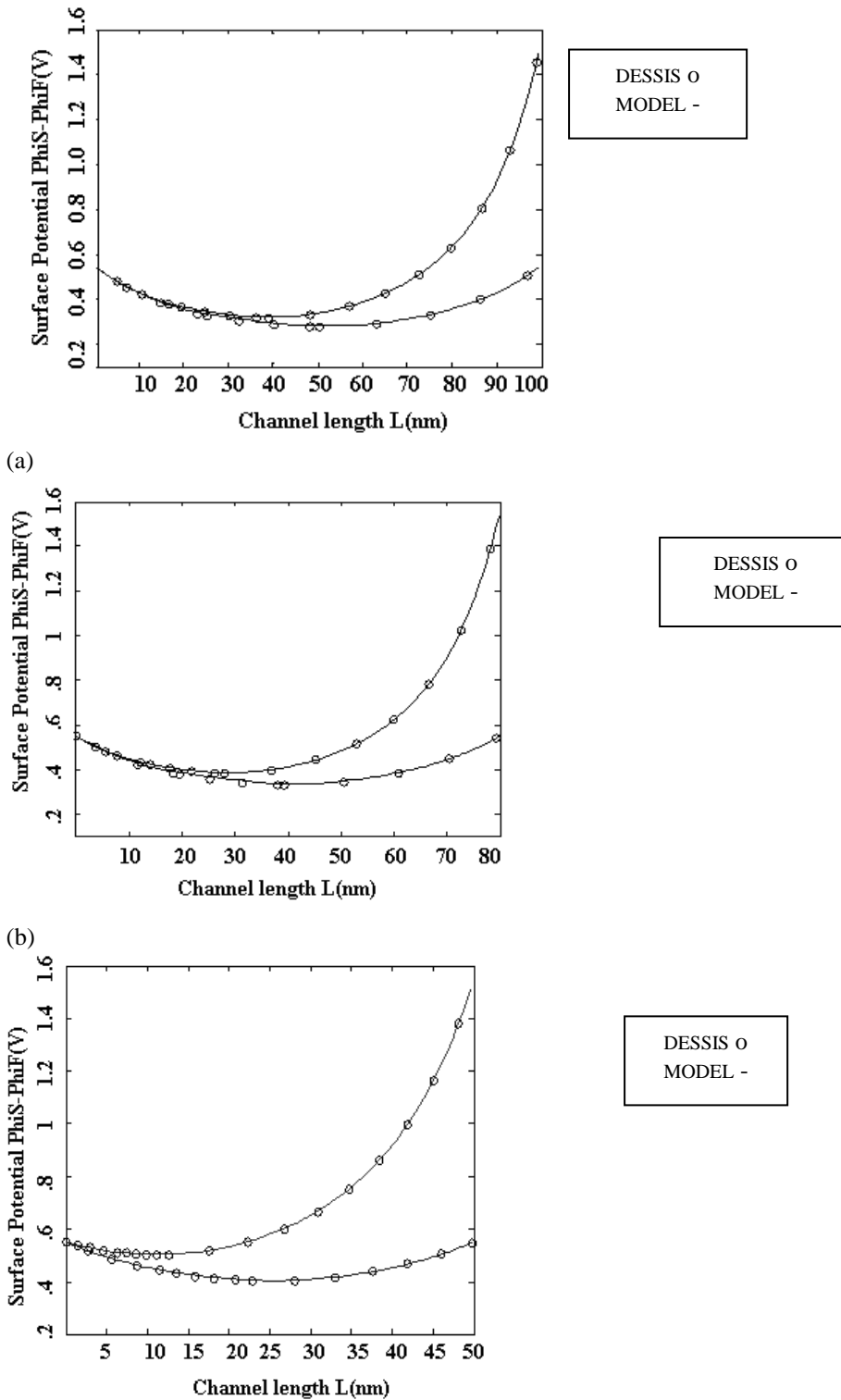
The channel is divided into five regions R_1, R_2, R_3, R_4, R_5 .

III RESULTS

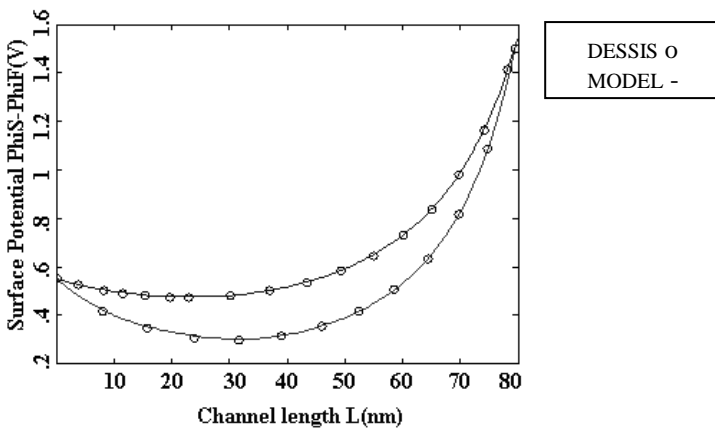
The MOSFET structure shown in Figure 1 is used to verify the surface potential model against the 2-D numerical device simulator DESSIS of ISE TCAD [1,2,3,4,5]. The concentration used for source and drain contacts are exactly the same as that of n^+ regions, so that the corresponding contact drops are exactly zero. The source, drain and gate are made of n -type polysilicon and the body contact is made of p -type polysilicon. We have plotted $(\Phi_s - \Phi_F)$, where Φ_s is the surface potential and Φ_F is the Fermi potential of the p -type substrate, versus the effective channel length. The effective channel length L is considered to be the length

from the source-channel metallurgical junction to the drain-channel metallurgical junction. The simulated data of the surface potential profile are extracted at a depth of around 0.5 nm from the bottom of the oxide layer. The channel doping concentration is denoted by N_a .

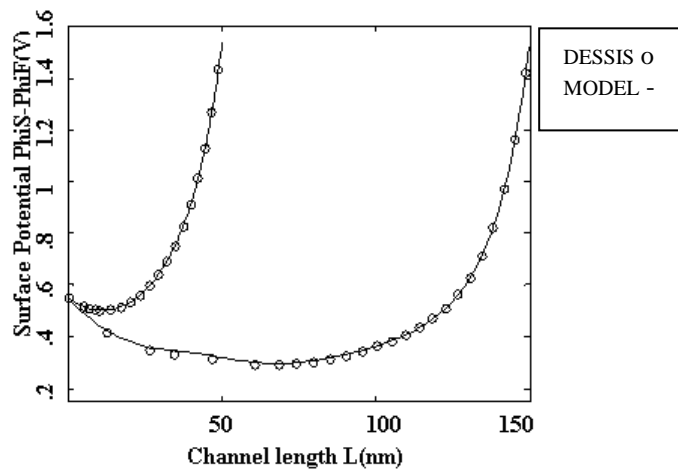
Figure 12 shows the surface potential profiles between the source and drain of a MOSFET for three different technology nodes (130-, 100-, and 70-nm nodes are used). The profiles for two different values of V_{DS} are shown for each of the technology nodes. N_a for all of the devices in Figure 12 is $6 \times 10^{17} \text{ cm}^{-3}$ while the gate and source bias voltages used are $V_{SB} = V_{GS} = 0 \text{ V}$. The values of the effective channel length L used are 100, 80, and 54 nm for the technology node of 130-, 100-, and 70-nm respectively.



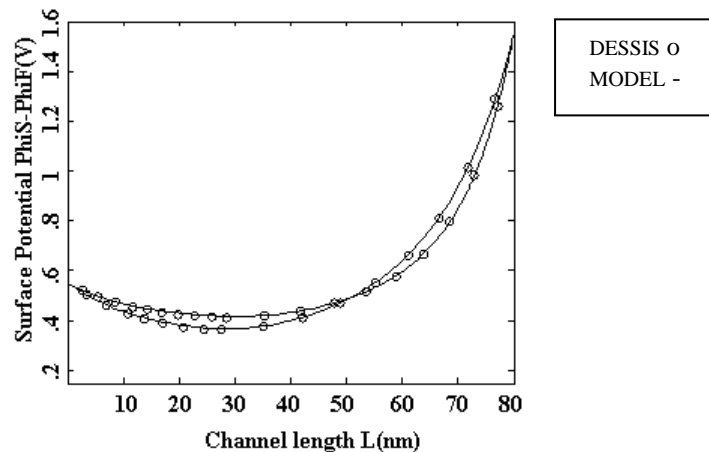
(a) Fig 12(a,b,c) Surface potential profiles for three different gate length MOSFETs. The substrate doping concentration is $N_a = 6 \times 10^{17} \text{ cm}^{-3}$ and bias voltages $V_{SB} = V_{GS} = 0 \text{ V}$ with two drain voltage; $V_{DS} = 0$ and 1 V are used. The technology nodes are (a) 130 -, (b) 100-, and 70 nm. PhiS= surface potential and PhiF=Fermi potential of the substrate.



(a)



(b)



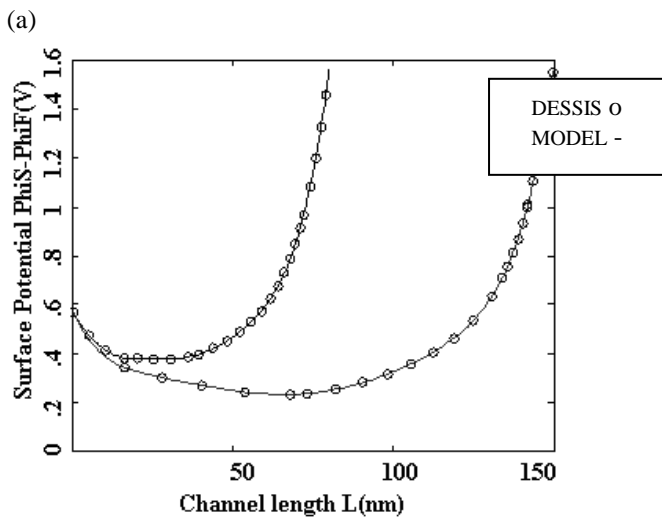
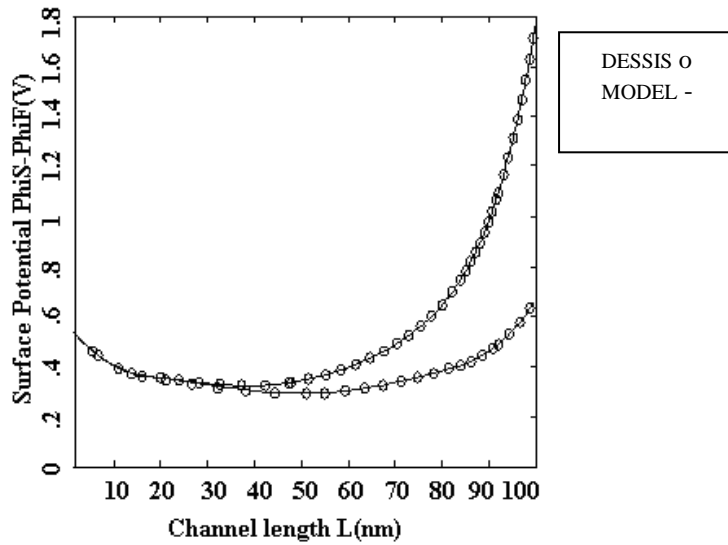
(c)

Fig 13 (a,b,c) Surface potential profiles for a device with $X_j = 30$ nm, $V_{SB} = V_{GS} = 0$ V and $V_{DS} = 1$ V. All other device parameters are same as the device in Fig 12 (b) except that (a) $N_a = 8 \times 10^{17} \text{ cm}^{-3}$ and $4 \times 10^{17} \text{ cm}^{-3}$ (b) $L = 100$ and 150 nm, and (c) $t_{ox} = 2$ and 4 nm.

As evident from Figure 13, a very good agreement of the proposed model (solid curve) with the DESSIS (circular symbols) is observed.

Our model is fairly accurate for wide variations of device parameters. In Figure 14(a) comparisons among the surface potential profiles obtained from our model and DESSIS for the same device as in Figure 13(b) is shown but with two other substrate concentrations $N_a = 8 \times 10^{17}$ and $4 \times 10^{17} \text{ cm}^{-3}$. As can be seen from Figure 14(a) also, our model agrees quite well with the DESSIS. The model is also verified against variation in channel length and oxide thickness next. It is very clear from Figure 14(b) and 14(c) that the agreement of our model with the DESSIS is very good for different channel lengths as well as oxide thicknesses. The accuracy of our model is obviously due to better modeling of the depletion layer thickness and introduction of inner fringing field.

The plots in Figure 15 are the subthreshold surface potential profiles in three different DH-MOS transistors for oxide thickness and junction depth values. All the plots in Figure 15 are for a pocket length $L_p = 16$ nm, pocket doping $N_p = 1.2 \times 10^{18} \text{ cm}^{-3}$ and substrate doping $N_a = 6 \times 10^{17} \text{ cm}^{-3}$, against the applied bias voltages $V_{SB} = 0$ V and $V_{GS} = 0$ V. Two different drain voltages $V_{DS} = 0.1$ and 1.2 V are used for the plots in Figure 15(a), while the plots shown in Figure 15(b) are for $V_{DS} = 1$ V. A very good agreement of our model with DESSIS is observed for the devices with different dimensions.



(a) Fig 14(a,b) Surface potential profiles with $L_p = 16$ nm, $N_p = 1.2 \times 10^{18} \text{ cm}^{-3}$, $N_a = 6 \times 10^{17} \text{ cm}^{-3}$ under applied bias $V_{SB} = V_{GS} = 0$ V in (a) 130-nm gate length device for $V_{DS} = 0.1, 1.2$ V, (b) 100- and 180-nm gate length devices for $V_{DS} = 1$ V. Effective channel length $L = 80, 100$ and 150 nm are used for 100-, 130-, and 180- nm devices respectively.

Substrate doping changed to $N_p = 1.8 \times 10^{18} \text{ cm}^{-3}$, $N_a = 9 \times 10^{17} \text{ cm}^{-3}$ and $N_p = 9 \times 10^{17} \text{ cm}^{-3}$, $N_a = 4 \times 10^{17} \text{ cm}^{-3}$ for $V_{SB} = V_{GS} = 0$ V, and $V_{DS} = 1$ V.

The proposed structure shown in Figure 7 is used to verify the DHDMG model against the 2-D numerical device simulator DESSIS. Two different metals M_1 and M_2 are used. The typical parameters for the oxide thickness, the junction depth and the channel length are $t_{ox} = 3.5$ nm, $X_j = 40$ nm and $L = 100$ nm which are representative for a typical 130-nm device, along with $V_{SB} = 0$ V are used. Similarly unless otherwise specified, equal values for L_1 and L_2 with typical work functions $W_1 = 4.25$ eV and $W_2 = 4.1$ eV are used in this study. Solid lines are used for the model predictions, while the circular symbols are used for the corresponding predictions by DESSIS.

Figure 15, 16 and 17 shows the comparison of the subthreshold surface potential profiles generated by our DHDMG model and the DESSIS, against the variation of the substrate and pocket doping.

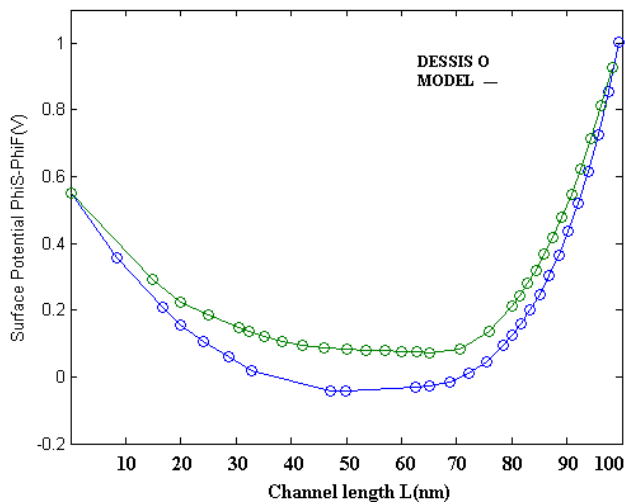


Fig15 The plots for DHDMG for two different values of the substrate doping $N_a=4 \times 10^{17}$ and $1 \times 10^{17} \text{ cm}^{-3}$ against the applied voltages $V_{GS}=0 \text{ V} = V_{GB} = V_{SB}$ and $V_{DS}=0.5 \text{ V}$.

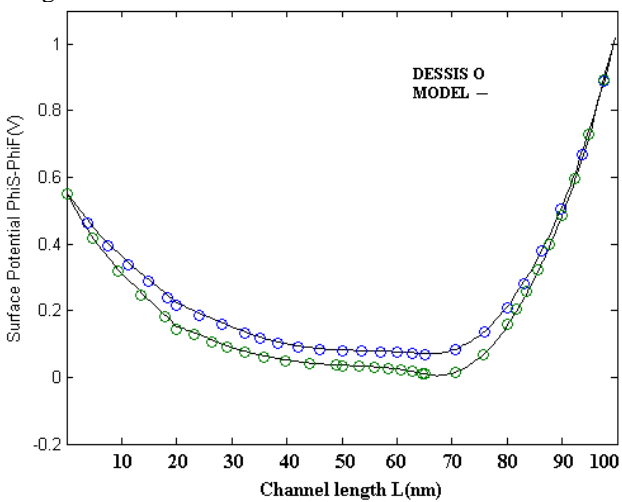


Fig 16 The plots of DHDMG for two different values of the pocket doping $N_p=1.2 \times 10^{18}$ and $1.8 \times 10^{18} \text{ cm}^{-3}$ against the applied voltages $V_{GS}=0 \text{ V} = V_{GB} = V_{SB}$ and $V_{DS}=0.5 \text{ V}$, $N_a=1 \times 10^{17} \text{ cm}^{-3}$ Φ_S = surface potential and Φ_F =Fermi potential of the substrate

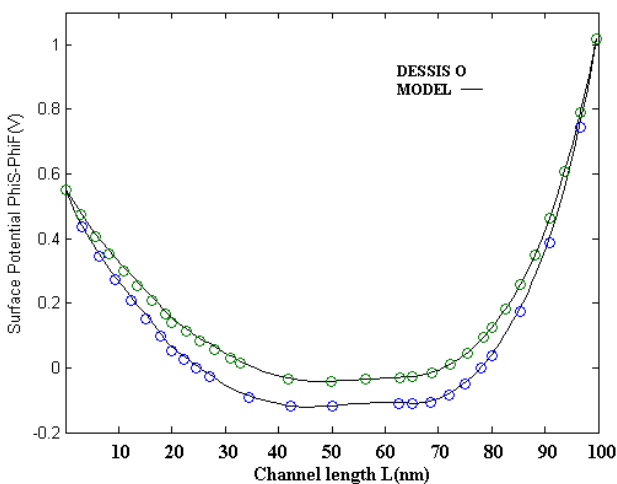


Fig 17 The plots for DHDMG for two different values of the substrate and pocket doping $N_p=1.8 \times 10^{18}$, $N_a=6 \times 10^{17} \text{ cm}^{-3}$ and $N_p=1.2 \times 10^{18}$, $N_a= 4 \times 10^{17} \text{ cm}^{-3}$ against the applied voltages $V_{GS}=0 \text{ V} = V_{GB} = V_{SB}$ and $V_{DS}=0.5 \text{ V}$. Φ_S = surface potential and Φ_F =Substrate Fermi potential

3.6 SUMMARY

An analytical subthreshold surface potential model for conventional short channel, Double halo and novel Double halo Dual Material Gate and Single halo Dual Material Gate MOSFETs have been proposed in this chapter that accounts for its dependence on varying depth along the channel depletion layer due to the source and the drain junctions. Again the fringing potentials due to inner fringing capacitances at the two ends of MOSFET are also considered for finding an accurate expression of the surface potential. The models can predict the subthreshold surface potential of the devices accurately for a wide variation of the device parameters such as the substrate concentration, the channel length, gate metals with different work functions and also for the different biasing conditions.

Our model is verified against the 2D device simulator DESSIS. A very good agreement of our model with results from DESSIS is obtained. The dependence of the surface potential on the junction depth is accommodated as per the scaling guide lines of ITRS roadmap. Therefore this model is very useful for circuit simulation and can be applied for analyzing the MOSFET amplifiers where the device is operated in the sub threshold region.

REFERENCES:

- [1] S. Baishya, A. Mallik and C. K. Sarkar, "A subthreshold surface potential model for short-channel MOSFET taking into account the varying depth of channel depletion layer due to source and drain junctions", IEEE Trans. Electron Devices, vol. 53, pp. 507-514, Mar. 2006.
- [2] S. Baishya, A. Mallik and C. K. Sarkar, "A subthreshold surface potential and drain current model for lateral asymmetric channel (LAC) MOSFETs", IETE Journal of Research, vol. 52, pp. 379 - 390, Sept-Oct. 2006.
- [3] S. Baishya, A. Mallik and C. K. Sarkar, "Subthreshold surface potential and drain current models for short-channel pocket implanted MOSFETs", Microelectronics Engineering. Available online.
- [4] Swapnadip De, A. Sarkar, N. Mohankumar, C. K. Sarkar "Effect of Fringing Field in Modeling of Subthreshold Surface Potential in Dual Material Gate (DMG) MOSFETs", Proceedings of ICECE 2008, vol.1, pp. 148-151, 20-22 December 2008, Dhaka, Bangladesh
- [5] A. Sarkar, Swapnadip De, N. Mohankumar, C. K. Sarkar, S. Baishya "Effect of Fringing Fields on Subthreshold Surface Potential of Channel Engineered MOSFETs; Proceedings of TENCON 2008, vol.1, pp.1-6, 19-20 November 2008, Hyderabad, India