Design of SRAM Memories with Different Topologies

[1]Nirmala S O, [2]Leela G H, [3]Aniket Vilas Vakude, [4]Dharani A S

[1,2]Associate Professor, [3,4]Student
Department of Electronics & Communicatiom Engineering,
Bapuji Institute of Engineering & Technology, Davangere, Karnataka, India

***Abstract*- This paper presents a comprehensive analysis of three static random access memory (SRAM) cell designs: 6T, 9T, and 10T. The purpose of the analysis is to determine the most suitable SRAM cell for attaining low power consumption and high-speed performance. Each cell design is evaluated based on various parameters, including write access time and power dissipation. The results obtained from the analysis provide valuable insights into the trade-offs between power consumption and performance, enabling the selection of an optimal SRAM cell for specific design requirements.**

***Keywords*- SRAM, 6T, 9T, 10T, low power consumption, high-speed performance.**

I. INTRODUCTION

Static random access memory (SRAM) plays a crucial role in modern digital systems, ranging from embedded devices to high-performance computing systems. As power consumption becomesa significant concern, SRAM cell design is considered a subject of intense research. This paper investigates the design and analysis of three different SRAM cells: 6T, 9T, and 10T. The objective is to identify the most suitable SRAM cell for attaining low power consumption and high-speed performance. This paper aims to provide a comprehensive comparative analysis of the 6T, 9T, and 10T SRAM cell topologies, evaluating their performance metrics under various operating conditions. By exploring parameters such as read and write stability, power consumption, area efficiency, access time, and noise tolerance, the study aims to shed light on thetrade-offs associated with each topology. The analyzed results will help designers in making proper decisions to optimize the performance and reliability of SRAM memories in future integrated circuits.

II. SRAM CELL DESIGNS

A. 6T SRAM Cell

The 6T SRAM cell is a widely used design due to its simplicity and compactness. It consists of six transistors arranged in a cross- coupled configuration as shown in Fig.1.

OPERATION

Read Operation: In the 6T SRAM cell, a read operation involves precharging the bit lines, activating the word line, evaluating the state of cell through the cross-coupled inverters, and sensing the voltage levels on the bit lines.

Write Operation: The write operation in the 6T SRAM cell involves activating the word line, driving the desired logic state onto the bit line, propagating the data through the cross-coupled inverters, and deactivating the word line to preserve the stored data.

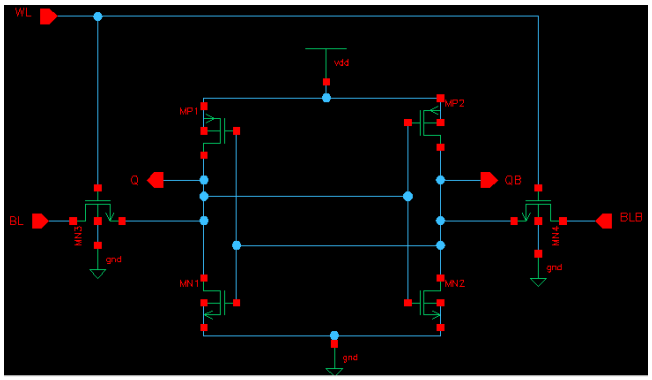

Fig 1: 6T SRAM cell

The 6T SRAM cell is widely used due to its simplicity, compactness, and good read/write performance. It provides a reasonable balance between density and performance.

B. 9T SRAM Cell

The 9T SRAM cell shown in Fig.2 is a popular design owing to its low leakage power consumption. It consists of nine transistors.

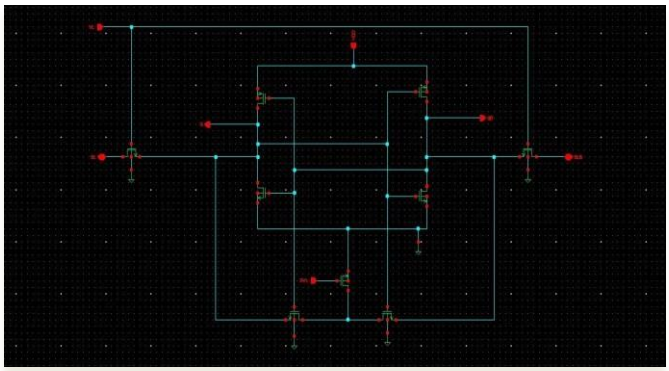

Fig 2: 9T SRAM cell

OPERATION

Read Operation: Like the 6T cell, the read cycle of the 9T SRAM cell involves precharging the bitlines and activating the wordline. However, the estimation of the cell state is performed using additional transistors, typically in the form of a read-assist circuit.

Write Operation: The write cycle in the 9T SRAM cell is comparable to the 6T cell, where the wordline is activated, and data is written onto the bitline. The additional transistors aid in improving write stability and reducing leakage power.

The 9T SRAM cell offers improved stability and less leakage power as against the 6T cell. It is particularly beneficial for low- power applications and scenarios where write robustness is crucial.

C. 10T SRAM Cell

The 10T SRAM cell shown in Fig.3 is another variation that aims to consider the stability issues encountered in the 6T cell while maintaining abalance between performance and power consumption. It consists of ten transistors.

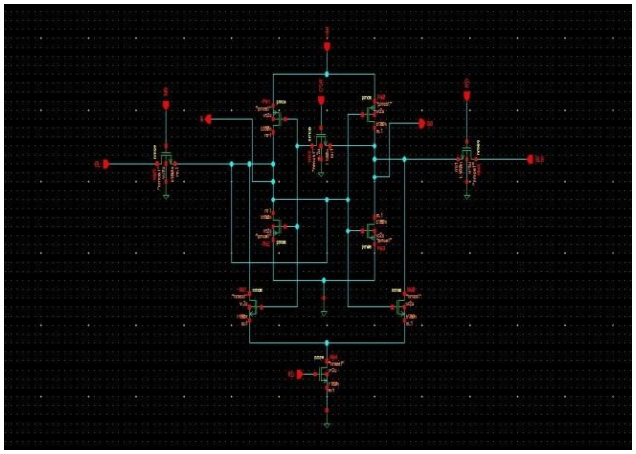

Fig 3: 10T SRAM cell

OPERATION

Read Operation: The read operation of the 10T SRAM cell involves precharging the bitlines, activating the wordline, evaluating the state of the cell through the cross-coupled inverters, and sensing the voltage levels on the bitlines. It is similar to the read operation of the 6T cell.

Write Operation: The write operation in the 10T SRAM cell is also same as 6T cell, with the wordline activation, data propagation through the inverters, and wordline deactivation. However, the additional transistors provide enhanced stability and reduced write disturbance.

The 10T SRAM cell addresses the stability issues encountered in the 6T cell while maintaining a balance between performance and power consumption. It offers improved write robustness and can besuitable for applications where both read and write reliability are crucial.

III. Analysis and Comparison

A. Write Access Time

The write access time is a critical performance metric for SRAM cells. It is defined as the time measured from the point at which WL (word line) reaches 50% of VDD to the point at which the storage node of the cell reaches 50% of VDD.

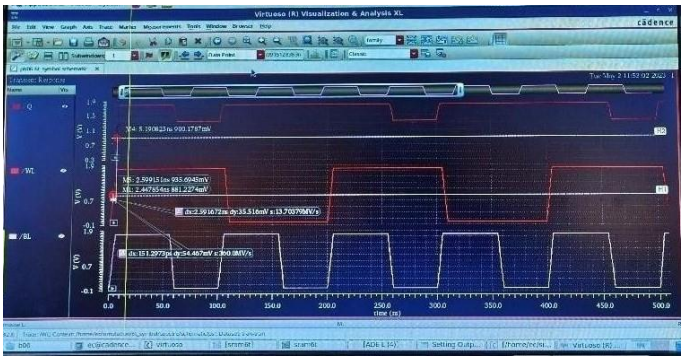

Fig 4: 6T Write access time

Fig 5: 9T Write access time

Table 1: write access time

	TECHNOLOGY	180nm(ps)
SRAM	6T	151.29
	9T	249.531

we have used the cadence virtuoso ADE (analog design environment) for carrying schematic design and analysis of SRAM cells. To design schematics of different SRAM cells we have used components from the library called gpdk180.

B. Power Dissipation

6T SRAM Cell

Static Power Dissipation: The 6T SRAM cell can have significantstatic power dissipation due to leakage currents flowing through the cross-coupled inverters, access transistors, and bitlines even when the cell is in standby mode.

Dynamic Power Dissipation: The dynamic power dissipation in the 6T SRAM cell is mainly associated with the charging and discharging of the bitlines during read and write operations. Itdepends on factors like frequency of access operations, data transitions, and bitline capacitance.

9T SRAM Cell

Static Power Dissipation: The 9T SRAM cell is so designed that it has less leakage power in comparison with 6T cell . By using additionaltransistors for read-assist or write-assist circuitry, the leakagecurrents can be reduced, leading to lower static power dissipation. **Dynamic Power Dissipation:** The dynamic power dissipation in the 9T SRAM cell is similar to the 6T cell since the core read andwrite operations are comparable. However, the additionaltransistors can slightly increase the dynamic power dissipation dueto their own switching activities

10T SRAM Cell

Static Power Dissipation: The 10T SRAM cell also aims to reduce leakage power compared to the 6T cell by incorporating additional transistors for improved stability. These additional transistors can help minimize leakage currents and reduce static power dissipation.

Dynamic Power Dissipation: Similar to the 6T and 9T cells, the dynamic power dissipation in the 10T SRAM cell is primarilyassociated with bitline charging and discharging during read and write operations. The additional transistors may slightly increase the dynamic power dissipation.

Table 2: Static Power Dissipation

	TECHNOLOGY	180nm
SRAM	6T	2.1929uW
	9T	1.978uW

IV. RESULTS

OUTPUT WAVEFORMS

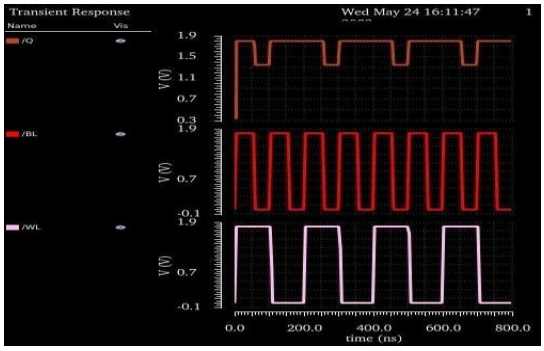

Fig 6: 6 T Write Operation

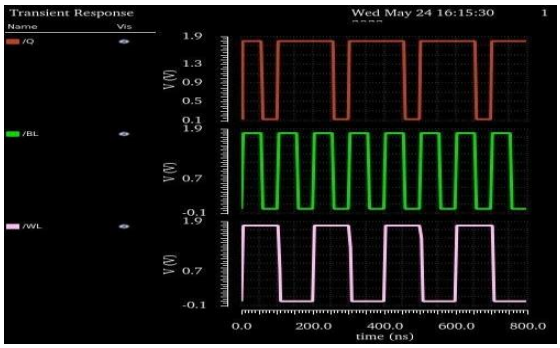

Fig 7: 9T Write Operation

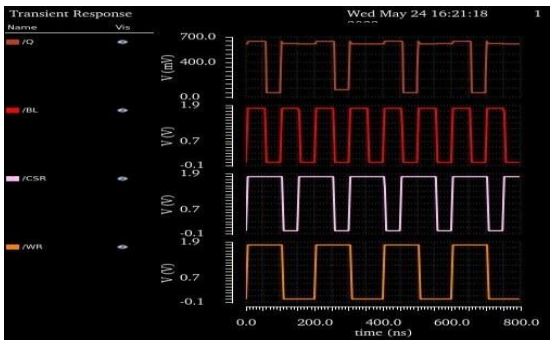

Fig 8: 10T Write Operation

The above waveforms in Fig. 6,7 & 8 are simulation outputs of 6T,9T and 10T SRAM cells.

CONCLUSION

The comparative analysis of 6T, 9T, and 10T SRAM cells presented in this paper offers good understanding of design considerations for achieving low power consumption and high- speed performance.

REFERENCES:

[1] Neil H. E. Weste, David Harris "CMOS VLSI Design : A circuits and systems perspective".
[2] Rabaey "Digital Integrated Circuits 2e".
[3] Ezeogu Chinonso Apollos Scholar, National Information Technology Development Agency,Nigeria. "Performance Analysis of 6T and 9T SRAM" International Journal of Engineering Trends and Technology. (IJETT) – Volume 67 Issue 4 - April 2019
[4] Prithu Jain, Shalabh Bansal, Vandana Khanna "Analysis of 6T SRAM Cell in Different Technologies" Volume 7 Issue 2 (2019) 133-135International Journal of Advance Research andInnovation.
[5] Ravi Hosamani Assistant Professor Electronics andCommunication Engineering, K.L.E. Institute of Technology,Hubli, India "Design and Analysis of 1-Bit SRAM" International Journal of Engineering Research & Technology (IJERT) Vol. 9Issue 09, September- 2020.
[6] Ashish Sachdeva, ECE Department, GLA University, Mathura,India. "Design of 10T SRAM cell with improved read performance and expanded write margin".