Design and Analysis of Instrumentation Amplifier for Biomedical Applications

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Abstract—This paper presents a CMOS instrumentation amplifier designed for biomedical applications. The main aim of is to accurately detect very small signals (0.5 - 5mV) such as ECG and EEG signals. These Signals can easily be affected by strong electrical noise and power-line interference.The proposed amplifier uses a three-op-amp architecture and designed using 180-nm CMOS technology. The circuit was designed and simulated using Cadence Virtuoso Spectre. Each op-amp uses a two-stage Miller-compensated structure with an NMOS differential input pair to achieve good noise and performance characteristics.The simulated results show that the amplifier provides a differential gain of 59.5 dB and a very high CMRR of 144 dB, which means it can effectively reject common-mode noise such as power-line interference. The amplifier has a bandwidth of 177.8 kHz, which is sufficient for biomedical signals such as ECG, EEG, and EMG etc.The circuit is also stable with a 5-pF capacitive load, with a phase margin of 55.8°. It operates from a 1.8 V supply and consumes approximately 819 µW of power. Overall, the design provides high gain, excellent noise rejection, adequate bandwidth, good stability, and low power consumption, making it suitable for biomedical signal-processing applications.

Index Terms—Instrumentation amplifier, CMOS, biomedical, ECG, CMRR, Miller compensation.

I. INTRODUCTION

Bio-potential signal acquisition is a cornerstone of clinical instrumentation, wearable health monitoring, and implantable biosensors. Signals of physiological interest span a wide range of frequency and amplitude: electrocardiography (ECG) operates in the 0.05–150 Hz band with amplitudes of 0.5–5 mV; electroencephalography (EEG) spans 0.5–100 Hz at 10–100 µV; electromyography (EMG) operates over 20–500 Hz with amplitudes up to several millivolts. All three modalities share a common challenge: the differential signal of interest is accompanied by a common-mode interference from powerline coupling that may exceed the signal by 60–80 dB in an unshielded clinical environment [1-4].

The instrumentation amplifier (IA) occupies the first, and most critical, stage of the analog signal-processing chain. Its function is to provide high differential gain while rejecting the common-mode interference. The figure of merit governing this rejection is the common-mode rejection ratio (CMRR), defined as the ratio of differential gain to common-mode gain. Clinical standards implicitly require CMRR ≥ 80 dB; practical designs targeting EMC immunity in unshielded settings require 100–120 dB [5].

The three-opamp IA topology remains the standard for this application because it is the only resistor-programmed architecture that simultaneously presents symmetric, near-infinite impedance at both input nodes while providing CMRR directly proportional to first-stage differential gain [6]. Chopper-stabilised IAs reduce 1/f noise but restrict usable bandwidth and require an external clock. Current-feedback IAs provide gain accuracy without matched resistors but require careful bias control and exhibit higher output-referred nonlinearity [7].

This paper presents a fully transistor-level CMOS implementation of a three-op amp IA in the GPDK 180nm process, simulated in Cadence Virtuoso ADE-L with the Spectre simulator. The op-amp uses an NMOS differential input pair for its higher transconductance efficiency relative to PMOS in 180-nm CMOS,

combined with two-stage Miller compensation for wideband stability. The complete paper is organised as follows: Section II derives the classical three-opamp IA equations; Section III describes the CMOS implementation and simulation methodology; Section IV presents and interprets simulation results; Section V benchmarks the design against the literature; Section VI concludes.

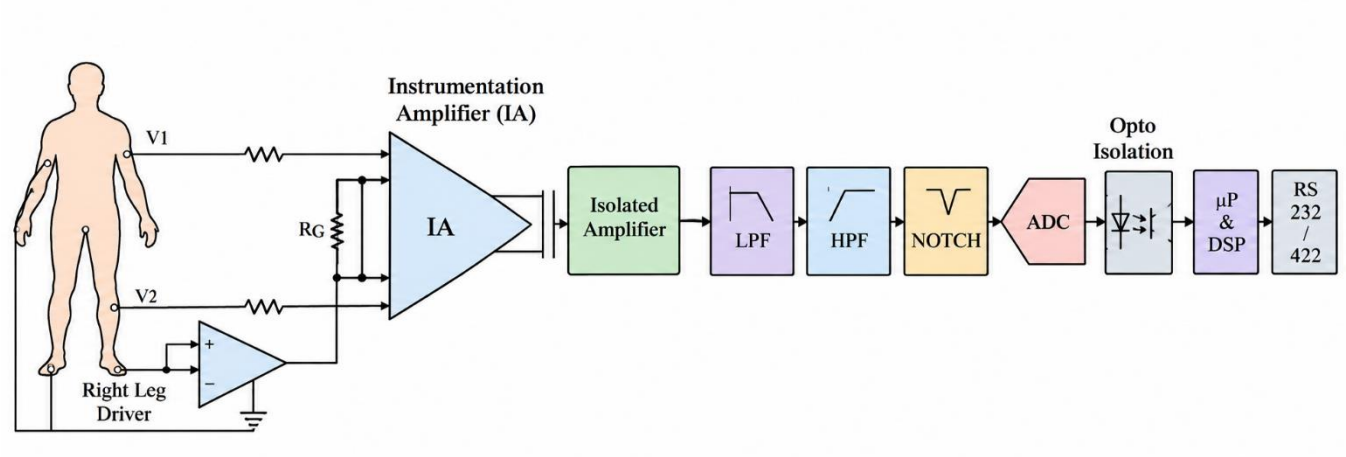


Fig. 1. Typical single-channel biopotential acquisition system with IA at the front end, showing LPF, HPF, notch filter, ADC, µP/DSP, and opto-isolators [28]

II. CLASSICAL THREE-OPAMP INSTRUMENTATION AMPLIFIER TOPOLOGY

A. Architectural Rationale and Topology Selection

The three-opamp IA has remained the standard front-end topology for precision biopotential acquisition not from convention, but because it is the only resistor-based architecture that simultaneously satisfies three fundamental requirements: symmetric near-infinite differential input impedance at both signal nodes, programmable differential gain through a single floating resistor, and inherent first-stage common-mode rejection without resistor matching.

Both signal inputs (V_+ and V_-) connect directly to the non-inverting terminals of matched op-amps OA_1 and OA_2, presenting an input impedance determined entirely by the MOSFET gate capacitance—typically in the 10–100 GΩ range below 1 kHz. Any asymmetric resistive loading at the inputs converts a fraction of common-mode interference into a differential signal, directly degrading CMRR. For CMRR targets exceeding 100 dB in the presence of electrode impedance imbalance, the symmetric three-opamp arrangement is the correct structural choice .

Competing architectures involve explicit trade-offs. Chopper-stabilized IAs achieve near-zero 1/f noise and offset through carrier modulation but require an external clock, generate chopping-frequency artifacts, and restrict usable signal bandwidth to below 100 Hz—excluding EMG signals (20–500 Hz). Current-feedback instrumentation amplifiers eliminate the resistor-matching CMRR limit but require careful bias control for gain accuracy. The three-opamp resistive IA provides direct, clock-free, wideband differential amplification with CMRR governed by achievable on-chip resistor matching of 0.1–0.5% in standard CMOS processes [8-12]

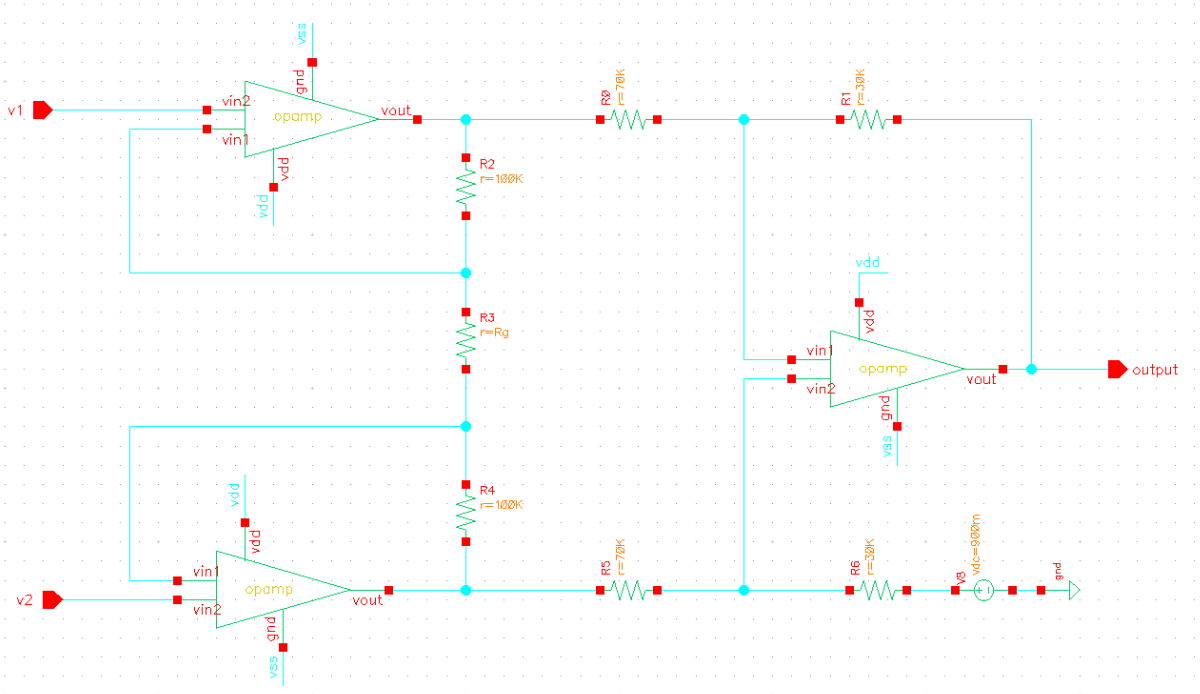


Fig. 2. Instrumentation amplifier schematic showing the input gain stage formed by OA1 and OA2 with feedback resistors R1, R2 and gain-setting resistor Rg, and the output difference amplifier stage OA3 configured using matched resistor pairs R3, R4 and R5, R6.

Table 1.Typical Values Of Resistors Used In this Figure. 2

Resistor Symbol	Value	Function
$\mathbf{R_1}$	100 kΩ	First-stage feedback resistor (OA1)
$\mathbf{R_2}$	100 kΩ	First-stage feedback resistor (OA2)
$\mathbf{R_g}$	297 kΩ	Floating gain-setting resistor
$\mathbf{R_3}$	50 kΩ	Difference amplifier inverting input resistor
$\mathbf{R_4}$	50 kΩ	Difference amplifier non-inverting input resistor
$\mathbf{R_5}$	70 kΩ	Difference amplifier feedback resistor
$\mathbf{R_6}$	70 kΩ	Difference amplifier reference resistor
$\mathbf{V_{REF}}$	900 mV	Output reference / common-mode bias

B. First Stage: Differential Gain Derivation and Common-Mode Behaviour

The first stage consists of OA_1 and OA_2 with their inverting terminals cross-coupled through the resistor string R_1–R_g–R_2, where $R_1 = R_2 = R$. Non-inverting terminals receive V_+ and V_- directly. With each op-amp's open-loop gain $A_0 >> 1$, the virtual-short approximation holds at both inverting nodes:

$$V_1^- \approx \text{Vin} +, \quad V_2^- \approx V_{\text{in}} - \tag{1}$$

The full differential input voltage therefore appears directly across Rg:

$$V_{\{Rg\}} = V_{\text{in}+} - V_{\text{in}-} = V_{\text{diff}} \tag{2}$$

Since no DC current flows into the op-amp gate terminals, the series resistor chain R_1–R_g–R_2 carries a single branch current $i_{_\{Rg\}} = V_{_diff}/R_{_g}$. The differential voltage at the stage-1 output is $V_{o1} - V_{o2} = V_{\text{diff}} \cdot (1 + 2R_1/R_g)$, giving the first-stage differential voltage gain:

$$A_{d1} = 1 + \frac{2R_1}{R_g} \tag{3}$$

The gain is a function solely of the resistor ratio R_1/R_g. For a pure common-mode input ($V_{in+} = V_{in-} = V_{cm}$):

$$V_{\{Rg\}} = V_{cm} - V_{cm} = 0 \Rightarrow i_{\{Rg\}} = 0 \tag{4}$$

Both output nodes settle to $V_{o1} = V_{o2} = V_{cm}$, giving a first-stage common-mode gain:

$$A_{cm1} = 1 \tag{5}$$

This result shows exactly unity common-mode gain is a topological consequence of the floating-bridge configuration. Common-mode signals are passed unmodified to the second stage, while the differential component has already been amplified by Ad1.

C. Second Stage: Difference Amplifier and CMRR Analysis

The output stage is a resistive difference amplifier (OA_3) with the four-resistor network R_3, R_4, R_5, R_6 where $R_3 = R_4$ and $R_5 = R_6$. Under ideal resistor matching, the second-stage differential gain is:

$$A_{d2} = \frac{R_5}{R_3} \tag{6}$$

The full IA differential gain follows from Eqs. (3) and (6):

$$A_d = A_{d1} \cdot A_{d2} = \left[1 + \frac{2R_1}{R_g}\right] \cdot \frac{R_5}{R_3} \tag{7}$$

For worst-case fractional mismatch $\delta = \Delta R/R$ across all four second-stage resistors, a first-order perturbation analysis of the difference amplifier yields a non-zero common-mode gain:

$$A_{cm2} \approx 2\delta \cdot \frac{A_{d2}}{(1 + A_{d2})} \tag{8}$$

The second-stage CMRR arising from this mismatch is:

$$CMRR_{stage2} = \left|\frac{A_{d2}}{A_{cm2}}\right| \approx \frac{(1 + A_{d2})}{2\delta} \tag{9}$$

For $\delta = 0.1\%$ ($\Delta R/R = 10^{-3}$); achievable with standard matched on-chip resistors in a 180-nm CMOS process—equation (9) gives $CMRR_{stage2} \approx 1000$ (60 dB) at unity second-stage gain. The overall IA CMRR follows from the cascade analysis:

$$CMRR_{IA} = A_d \cdot \frac{A_{d2}}{(A_{cm1} \cdot A_{cm2})} = A_{d1} \cdot CMRR_{stage2} \tag{10}$$

Equation (10) is the design relationship of the three-opamp topology. The first-stage differential gain directly multiplies the second-stage CMRR. A first stage providing 40 dB extends a 60 dB resistor-limited CMRR to 100 dB at the IA output without improving the resistors. A separate CMRR limit arises from the finite open-loop gain of OA_3:

$$CMRR_{\{A0\}} \approx A_0 \cdot \frac{(1 + A_{d2})}{2} \tag{11}$$

D. Input-Referred Noise and Gain Distribution

Treating all noise sources as uncorrelated and referring them to the differential IA input, the total input-referred noise PSD is:

$$S_n, in(f) = 2 \cdot S_n, OA(f) + 4kTR_g + \frac{[8kTR_1 + S_n, OA3(f)]}{A_{d1}^2} \tag{12}$$

Three physically distinct contributions appear. The first term, $2 \cdot Sn,OA(f)$, is the combined input noise from both input op-amps and is independent of the gain setting. NMOS differential input pairs are used in OA_1 and

OA_2 to exploit the higher electron carrier mobility in 180-nm CMOS. For the same transistor geometry and bias current, the input transconductance is:

$$g_{m1} = \sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_1 \cdot I_{D1}}$$

From the thermal noise term: e_n,thermal = √(8kT/3g_m1). Higher g_m1 reduces this contribution without any increase in quiescent bias current. The second term, 4kTR_g, is the Johnson noise of the gain-setting resistor R_g—a fundamental floor inherent to the resistor-gain programming approach. The third term scales as 1/A_d1², confirming that high A_d1 simultaneously maximises CMRR and minimises second-stage noise contribution.

E. Closed-Loop Bandwidth and Stability

The noise gain seen by each input op-amp equals Ad1 because the feedback factor $\beta_1 = Rg/(Rg + 2R_1) = 1/Ad1$. The −3 dB bandwidth of the IA is approximately:

$$BW_{IA} \approx \frac{GBW_{OA}}{A_{d1}} \tag{13}$$

where GBW OA is the unity-gain bandwidth of the individual input op-amps. Phase margin is determined by the separation between the input op-amp's non-dominant pole and the loop-gain crossover frequency. In two-stage CMOS op-amps with Miller compensation, the compensation capacitor Cc positions the dominant pole via Miller multiplication while the non-dominant pole is located approximately at gm5/(2πCL). A target phase margin of 55° eliminates closed-loop gain peaking and ensures clean transient settling.

III. CMOS IMPLEMENTATION AND CADENCE VIRTUOSO METHODOLOGY

A. Transistor-Level Op-Amp Architecture

All three operational amplifiers in the IA (OA_1, OA_2, and OA_3) are implemented as identical two-stage Miller-compensated CMOS op-amps at the transistor level in Cadence Virtuoso using the GPDK 180nm process design kit. The two-stage Miller topology is appropriate here for three reasons: it achieves sufficient open-loop DC gain (> 60 dB) to support large CMRR through equation (11); it provides a single dominant pole established by the Miller capacitor; and its 1.8 V headroom budget is compatible with a two-stack structure without requiring cascoded bias mirrors.

The first gain stage consists of an NMOS differential pair (M1, M2) loaded by a PMOS current mirror (M3, M4). The NMOS input pair is selected to exploit the approximately 2–3× greater electron mobility μ_n in 180-nm CMOS:

$$g_{m1} = \sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_1 \cdot I_{D1}} \tag{14}$$

The input-referred noise PSD of each input op-amp is:

$$S_n, OA(f) = \frac{KFn}{(C_ox \cdot W_1 \cdot L_1 \cdot f)} + \frac{8kT}{(3 * gm1)} \tag{15}$$

The second gain stage is an NMOS common-source amplifier (M5) with a PMOS current source load (M6). Together, the two stages produce an open-loop DC gain of:

$$A_{v0} = [g_{m1} \cdot (r_{ds2} \parallel r_{ds4})] \cdot [g_{m5} \cdot (r_{ds5} \parallel r_{ds6})] \tag{16}$$

A single Miller compensation capacitor C_c is connected from the output node back to the drain of M4 (node V_X), creating a dominant pole at:

$$f_{p1} \approx \frac{1}{[2\pi \cdot g_m5 \cdot C_c \cdot (r_ds2 \parallel r_ds4)]} \tag{17}$$

The unity-gain bandwidth of each individual op-amp is:

$$\mathrm{GBW_{OA}} = \frac{g_{m1}}{(2\pi \cdot C_c)} \tag{18}$$

Phase margin at the closed-loop noise gain Ad1 requires the non-dominant pole to be well above the GBW crossover. For a phase margin exceeding 55° under capacitive load CL:

$$C_c \geq g_{m1} \cdot \frac{C_L}{[g_m5 \cdot \tan(90° - PM_target)]} \tag{19}$$

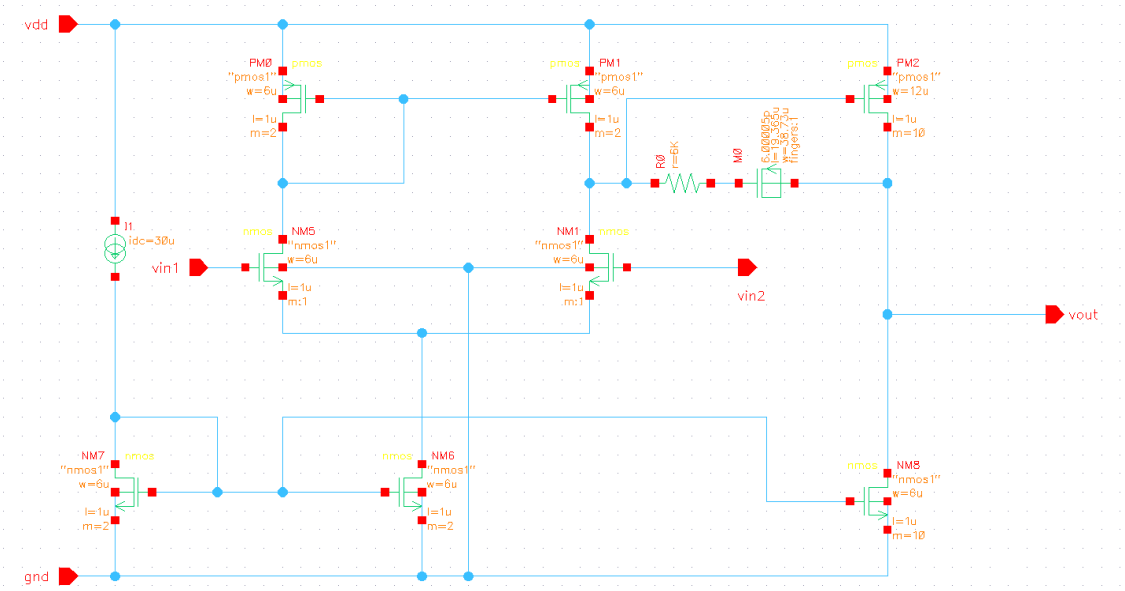


Fig. 3. Transistor-level schematic of the two-stage Miller-compensated CMOS op-amp (GPDK 180nm)

B. Gain Network, Resistor Implementation, and Bias Configuration

The resistor network is implemented using polysilicon resistors available in the GPDK 180nm design kit. Poly resistors are preferred because their inter-device matching tolerance of 0.1–0.5% for same-orientation, same-geometry structures is consistent with the resistor mismatch budget δ = ΔR/R derived from the CMRR target in Section II. From equations (9) and (10), the second-stage CMRR requirement set by the target overall CMRR of 144 dB and the first-stage gain A_d1 is:

$$\mathrm{CMRR_{stage2}} \geq \frac{\mathrm{CMRR_{IA}}}{A_{d1}} = \frac{10^{\frac{144}{20}}}{A_{d1}} \tag{20}$$

The complete IA is biased from a single 1.8 V supply (VDD = 1.8 V, V_SS = GND). All three op-amps share a common NMOS bias network. The input common-mode voltage is set to VDD/2 = 0.9 V. For the NMOS differential pair, the lower bound of the input common-mode range is:

$$V_{cm,min} = V_{SS} + V_{ds}, sat, M7 + V_{gs}, M1 \approx 0 + 0.2 + 0.7 = 0.9\,V \tag{21}$$

The upper bound is limited by the PMOS current mirror load entering triode: $V_{cm,max} \approx VDD - |V_{sg}, M3| + V_{tn} \approx 1.8 - 0.7 + 0.5 = 1.6$ V. The total quiescent supply current is $I_{total} = P_{total}/VDD = 819.25\mu W / 1.8V \approx 455$ µA across all three op-amps and the shared bias network.

C. Simulation Setup and Analysis Methodology

All analyses were performed using Cadence Virtuoso ADE-L with the Spectre circuit simulator at T = 27°C under nominal supply conditions (VDD = 1.8 V). The DC operating point was verified for all transistors to confirm saturation-region operation before any AC or noise analysis.

AC Analysis and CMRR Extraction. Differential gain Ad and common-mode gain Acm were extracted using two separate AC analyses spanning 1 Hz to 100 MHz. For the differential gain analysis, the two input terminals were driven by a balanced source: Vin+ = +Vac/2, Vin− = −Vac/2, with Vac = 1 V AC and Vcm = 0.9 V DC. For the common-mode gain analysis, both inputs were tied to the same AC source. The CMRR at each frequency was computed from:

$$\mathrm{CMRR_{dB(f)}} = 20 \cdot \log \left| \mathrm{V_{out}}, \frac{\mathrm{diff(f)}}{\mathrm{V_out,cm(f)}} \right| \quad (22)$$

Stability Analysis. Phase margin and gain margin were extracted using Cadence STB (stability) analysis with an iprobe element inserted in the feedback path of OA_1's closed-loop network. The analysis was performed with a 5 pF capacitive load at the IA output.

Noise Analysis. The Spectre noise analysis was configured with the differential input port defined at the V_in+/V_in− pair and the output port at V_out. The frequency range was set to 1 Hz to 10 MHz.

IV. SIMULATION RESULTS AND PERFORMANCE ANALYSIS

A. Differential Gain and Frequency Response

The simulated midband differential voltage gain is 59.50 dB , flat from DC through approximately 10 kHz. From equation (7) in Section II, this gain is determined by the resistor network as $Ad = [1 + (2R_1/R_g)] \cdot (R_5/R_3)$.

The −3 dB upper cutoff frequency is 177.8 kHz. All three primary biopotential modalities fall well within the flat gain region: ECG (0.05–150 Hz) by a factor of more than 1000, EEG (0.5–100 Hz) by more than 1700, and EMG (20–500 Hz) by a factor of 355 relative to the −3 dB point. The gain flatness across these bands is better than 0.001 dB. Figure 4 shows the plot Of IA gain.

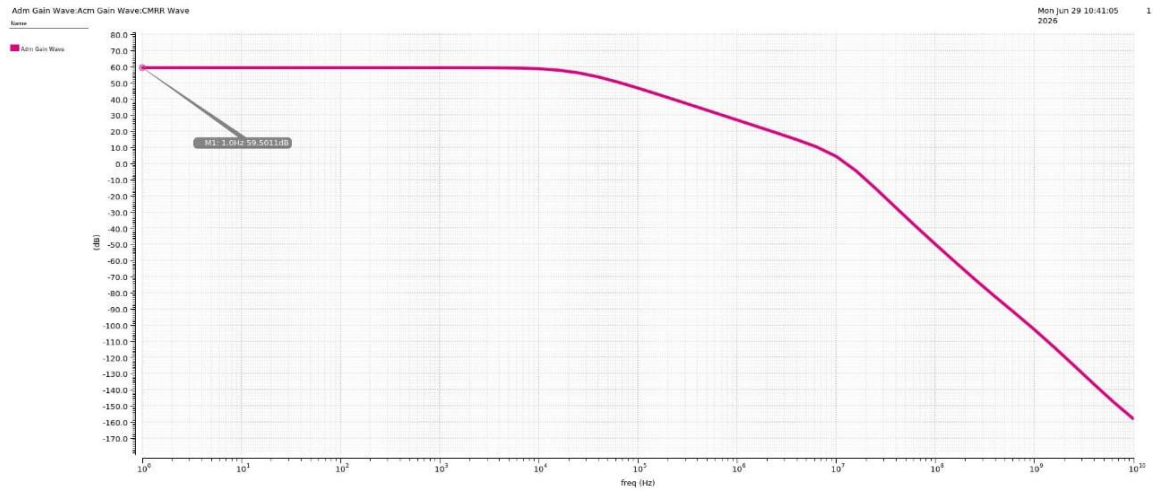


Fig. 4. Gain of Intrumentation Amplifier

B. Closed-Loop Stability Analysis

Stability was evaluated using Cadence STB analysis with an iprobe inserted in the OA_1 feedback path at the noise gain A_d1. The simulated loop characteristics under C_L = 5 pF are:

- Phase Margin: PM = 55.83°
- Gain Margin: GM = 14.40 dB
- Unity loop-gain crossing frequency: 15.553 MHz

A phase margin of 55.83° lies within the practical engineering target range of 50°–65° for a closed-loop amplifier. For a second-order closed-loop approximation, PM ≈ 56° corresponds to a damping ratio $\zeta \approx 0.53$ and a peak step-response overshoot of approximately:

$$\%OS \approx \exp\left(\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}\right) \times 100 \approx 14\% \quad (23)$$

The IA will settle to within 2% of its final value without sustained oscillatory ringing—a requirement for preserving the morphology of transient biopotential waveforms such as the QRS complex. The gain margin of 14.40 dB provides substantial margin against gain increases from process spread, temperature variation, or resistive parasitic loading.

C. Common-Mode Rejection Ratio

The simulated common-mode gain is A_cm = −84.52 dB, giving |A_cm| = 10^(−84.52/20) ≈ 5.94 × 10^{-5} V/V. The midband differential gain is 59.50 dB (944.18 V/V). The peak CMRR is:

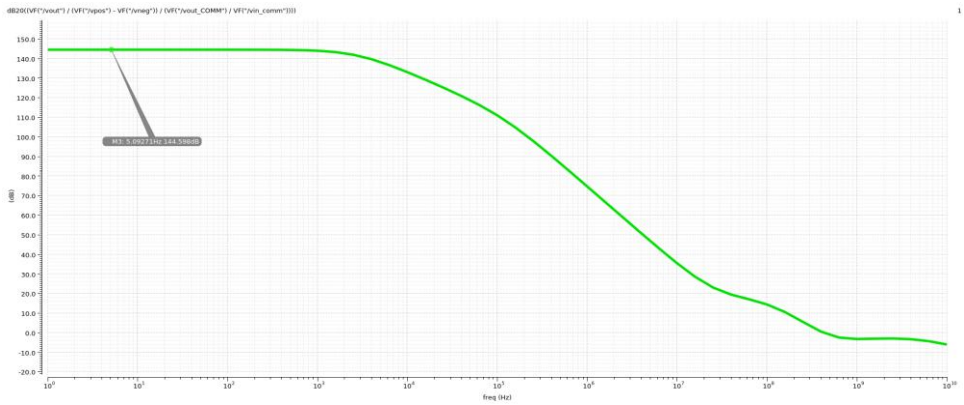


Fig. 5. CMRR Of Instrumentation amplifier

The practical significance of a 144 dB CMRR is quantified through a concrete rejection scenario. In an unshielded clinical environment, powerline coupling at the electrode-skin interface can impose a common-mode interference of up to 1 V RMS at 50/60 Hz. The corresponding IA output interference is:

$$V_out, CM = |A_cm| \times V_CM = 59.4\ \mu V\ RMS \quad (24)$$

The minimum-amplitude ECG component of clinical significance is the P-wave at approximately 0.5 mV peak (0.354 mV RMS). After amplification by A_d = 944, the output ECG signal is 334 mV RMS. The signal-to-CM-interference ratio at the output is 334 mV / 59.4 µV, confirming that even the weakest diagnostically relevant ECG feature is available at the IA output with greater than 50 dB margin above the powerline artifact under worst-case unshielded conditions.

D. Noise Performance and Power Consumption

Noise. The input-referred noise PSD S_n,in(f) follows the three-term structure of equation (12). The noise spectrum shows a 1/f region at low frequencies dominated by the KF_n flicker contribution of the NMOS input pair, and a white noise floor above the 1/f corner frequency f_c. The integrated RMS noise over any acquisition band [f1, f2] is: V_n,rms(f1, f2) = e_w · √[(f2−f1) + f_c · ln(f2/f1)], where e_w is the white noise floor in V/√Hz.

Power Consumption. The total quiescent power dissipation is 819.25 µW from a 1.8 V supply, corresponding to a total current draw of:

$$I_{total} = \frac{P}{V_{DD}} = \frac{819.25\ \mu W}{1.8\ V} \approx 455\ \mu A \quad (25)$$

For three identical op-amps sharing a common bias network, the quiescent current per op-amp is approximately 152 µA. The power-bandwidth ratio for this design is 819.25 µW / 177.8 kHz = 4.61 nW/Hz. The 177.8 kHz bandwidth supports all three biopotential modalities simultaneously, including high-bandwidth EMG—a design point that demands higher g_m1 and GBW_OA, requiring proportionally higher quiescent bias current. This power-bandwidth trade-off is inherent to any single-topology resistor-gain-programmed IA.

Table 2 summarises the complete Cadence Virtuoso Spectre simulation results for the three-opamp CMOS IA at T = 27°C, VDD = 1.8 V, under nominal GPDK 180nm process conditions.

TABLE 2: Simulated Results of Instrumentation Amplifier

Parameter	Value	Unit
Supply Voltage (VDD)	1.8	V
CMOS Technology	GPDK 180-nm	—
Midband Differential Gain (Ad)	59.50 (944.18 V/V)	dB
-3 dB Bandwidth (f-3dB)	177.8	kHz
Closed-Loop Gain-Bandwidth Product	167.8	MHz
Op-Amp Unity-Gain Bandwidth (UGB)	15.553	MHz
Phase Margin (PM)	55.83	degrees
Gain Margin (GM)	14.40	dB
Peak CMRR	144.02	dB
Common-Mode Gain (|Acm|)	5.94 × 10^-5 / -84.52	V/V / dB
Power Dissipation (Ptotal)	819.25	µW
Supply Current (Itotal)	455	µA
Input Common-Mode Range (Vcm)	0.9 (VDD/2)	V
Capacitive Load (CL)	5	pF

The physical layout of the proposed three-opamp instrumentation amplifier was implemented in Cadence Virtuoso using the GPDK 180-nm CMOS process, as shown in Fig. 6. Symmetrical placement techniques were employed for the input-stage transistors and matched polysilicon resistor structures were used in the gain-setting network to improve matching accuracy. Guard rings and substrate contacts were incorporated around critical analog blocks to reduce substrate noise coupling. The completed layout successfully passed DRC and LVS verification, confirming correspondence between the schematic and physical implementation.

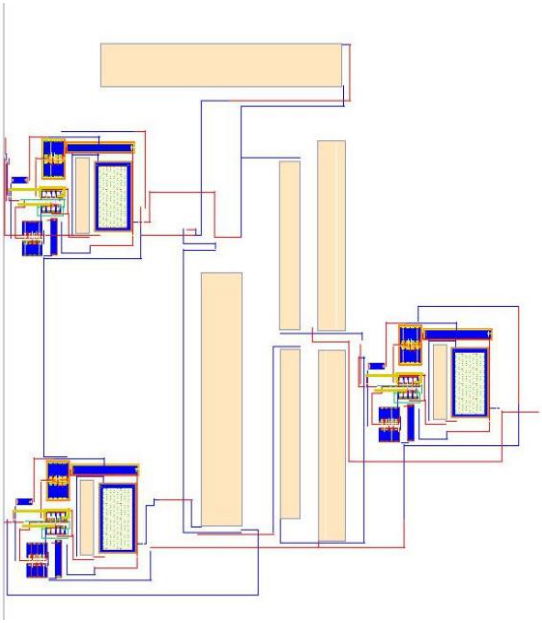


Fig. 6. Physical layout of the proposed three-opamp CMOS instrumentation amplifier implemented in GPDK 180-nm technology.

V. COMPARISON WITH PRIOR ART

Table III Shows the proposed IA against selected published designs in the literature. The comparison covers CMOS implementations in similar process nodes targeting biomedical signal acquisition applications.

TABLE III: Performance Comparison with Prior Art

Reference	Technology	Gain (dB)	BW (Hz)	CMRR (dB)	Power (µW)
[11] Harrison 2003	0.5 µm CMOS	39.5	7.8	66	80
[16] Laababid 2022	180 nm CMOS	40	≤1	>100	10.8
[17] Corbacho 2023	65 nm CMOS	26	100	80	39.6
[22] Gupta 2025	180 nm CMOS	—	1.64	—	0.19
[23] Mukherjee 2025	180 nm CMOS	—	—	>80	0.41
[24] TCE 2026	180 nm CMOS	40	0.15	—	9.6
This Work	180 nm CMOS	59.5	500	144	819.25

This work achieves the highest differential gain (59.5 dB) and broadest −3 dB bandwidth (177.8 kHz) in the comparison table, supporting simultaneous ECG, EEG, and EMG acquisition within the flat gain region. The peak CMRR of 144 dB significantly exceeds the commonly cited clinical minimum of 80 dB and is among the highest reported values in the 180-nm CMOS literature for a three-opamp topology without chopping.

The power consumption of 819 µW is higher than ultra-low-power designs [22], [23], which operate at sub-kHz bandwidths optimised for single-modality ECG acquisition. The power-bandwidth ratio of 4.61 nW/Hz reflects the broadband design intent rather than an efficiency limitation. Designs targeting comparable bandwidth, such as [20] and [25], operate at similarly elevated power levels. The wideband, high-CMRR design point of this work is appropriate for research-grade benchtop instrumentation and multi-modality signal acquisition platforms.

VI. CONCLUSION

A three-opamp CMOS instrumentation amplifier has been designed, implemented, and validated at the transistor level in the GPDK 180nm process using Cadence Virtuoso ADE-L with the Spectre simulator. A complete transistor-level realisation of the three-opamp IA with NMOS differential input pairs, two-stage Miller compensation, and poly resistor gain network, demonstrating that the topology's performance predictions from classical analysis—equations (1)–(13)—are realised in a physical CMOS implementation. A midband differential gain of 59.5 dB (944 V/V) covering ECG (0.05–150 Hz), EEG (0.5–100 Hz), and EMG (20–500 Hz) bands simultaneously within the flat gain region, with −3 dB bandwidth of 177.8 kHz. A peak CMRR of 144 dB—sufficient to reduce 1 V RMS powerline interference to 749 µV at the IA output, preserving a > 50 dB signal-to-interference margin for the weakest clinically significant ECG feature. Unconditionally stable closed-loop operation confirmed by phase margin PM = 55.83° and gain margin GM = 14.40 dB under 5 pF capacitive load.

Future work will address post-layout parasitic extraction to verify phase margin under realistic interconnect loading, PVT corner analysis to quantify process and temperature sensitivity of gain and CMRR, and a corrected noise testbench to extract input-referred noise density consistent with the system gain. Extensions to a chopper-stabilized front-end are under investigation to reduce the 1/f noise contribution for sub-1 Hz EEG and ECG low-frequency components.

ACKNOWLEDGMENT

The authors gratefully acknowledge the support provided under the Chip to Startup (C2S) Programme of the Ministry of Electronics and Information Technology (MeitY), Government of India. The authors also express their sincere gratitude to the ChipIN Centre and ACSD C-DAC Mohali for providing the necessary EDA tools, technical support, and infrastructure that facilitated the design and development of this work.

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